Latest Advancements in Motor Hardware-In-the-Loop Simulation (HILS) based on JMAG-RT

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Abstract :

Motor HILS (Hardware-in-the-loop simulator) has been recognized for many years now as an essential design and testing tool of motor drives, for increased product reliability, shorter time to market and lower total design cost. However, there remained many needs of the motor HILS to be addressed. Among these needed features are: more accurate models, more powerful simulators with distributed processing, etc.

Finite-Element Analysis based motor HILS, resulting from the integration of JMAG-RTR tool with RT-LABR simulator, addresses and fulfills these requirements. JMAG-RT-based Motor HILS of a complete permanent magnet synchronous motor drive can be conducted today on RT-LAB HILS at sub-microsecond time steps on powerful new FPGA resulting in unprecedented simulation accuracy.

And the integration with multi-processor platform yields a full motor HILS with high accurate motor model, ultra-fast drive simulation and distributed multi-rate simulation enabling the integration of other parts of the designed system (electrical, mechanical, hydraulic, etc), for a complete system HILS.

The presentation discusses all these items and describes the latest advancements in motor HILS.

Latest Advancements in Motor Hardware-In-the-Loop Simulation (HILS) based on RT-LAB & JMAG-RT

JMAG Users Conference 2010

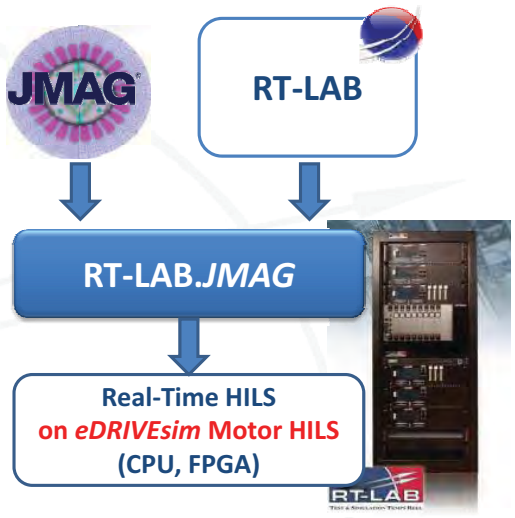
Simon Abourida

Date: 2010-11-10

OPAL-RT

Abstract

- Motor HILS (Hardware-in-the-loop simulation)
- Integration of JMAG-RT® tool with RT-LAB® HILS simulator
  → motor HILS at ~ 1 us
- All types of **faults** on the motor drive supported (open/short-circuit)
- Multi-processor HILS platform
  → a *large system HILS*



Outline

A. Overview

- Introducing Opal-RT
- Hardware-In-the-Loop Simulation → RT-LAB
- Finite-Element Analysis → JMAG-RT
- JMAG-RT & RT-LAB

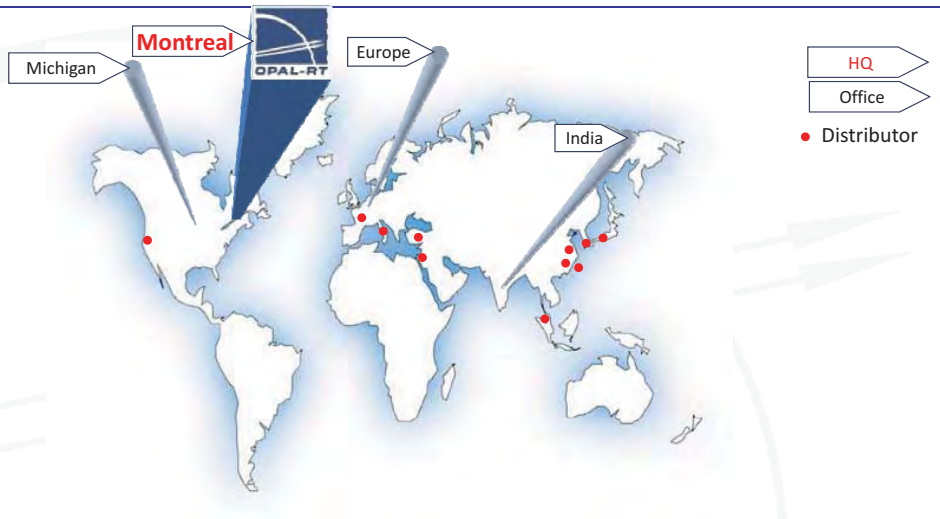
B. Latest Advancements

- FPGA-based Motor HILS
- Features
- Fault modes
- HILBox OP5600

Latest Advancements in Motor Hardware-In-the-Loop Simulation (HILS) based on RT-LAB & JMAG-RT

A. OVERVIEW

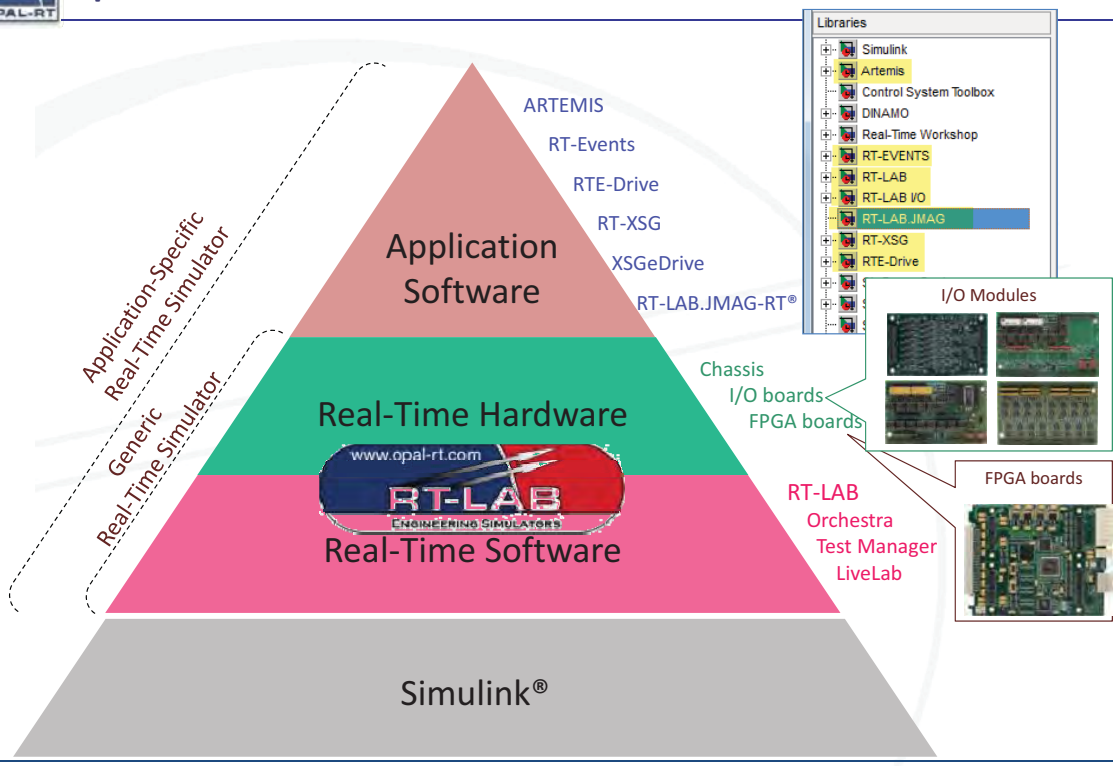
Introduction of Opal-RT



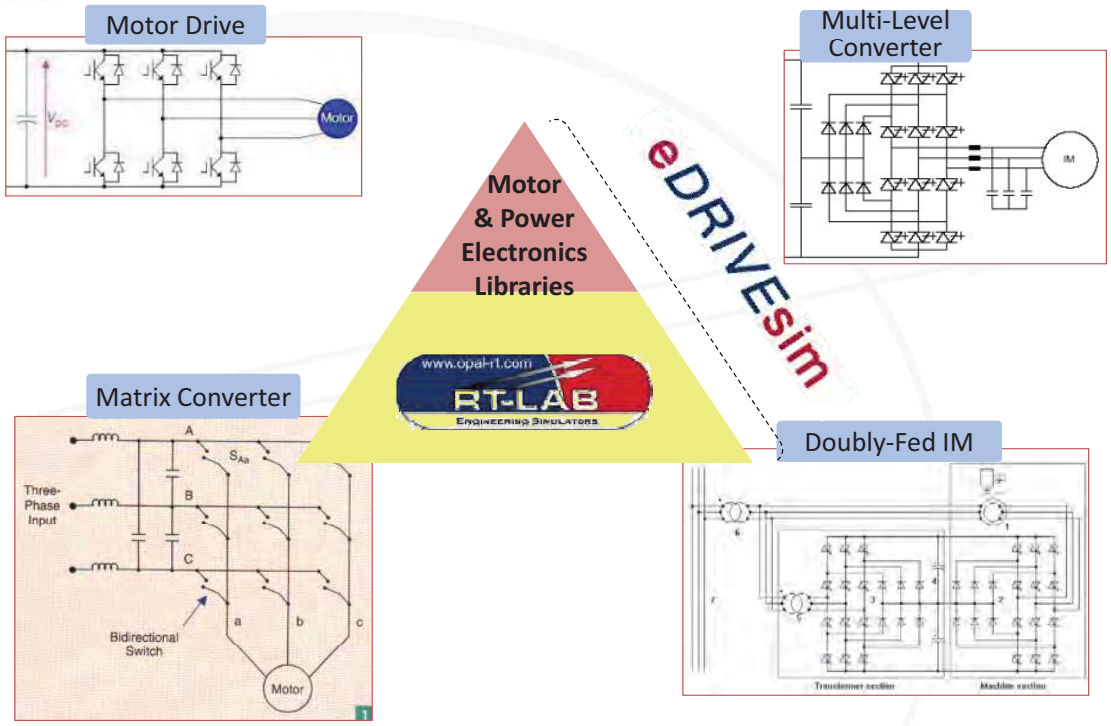
Real-Time Digital Simulators

Rapid Control Prototyping
Hardware-In-the-Loop simulation

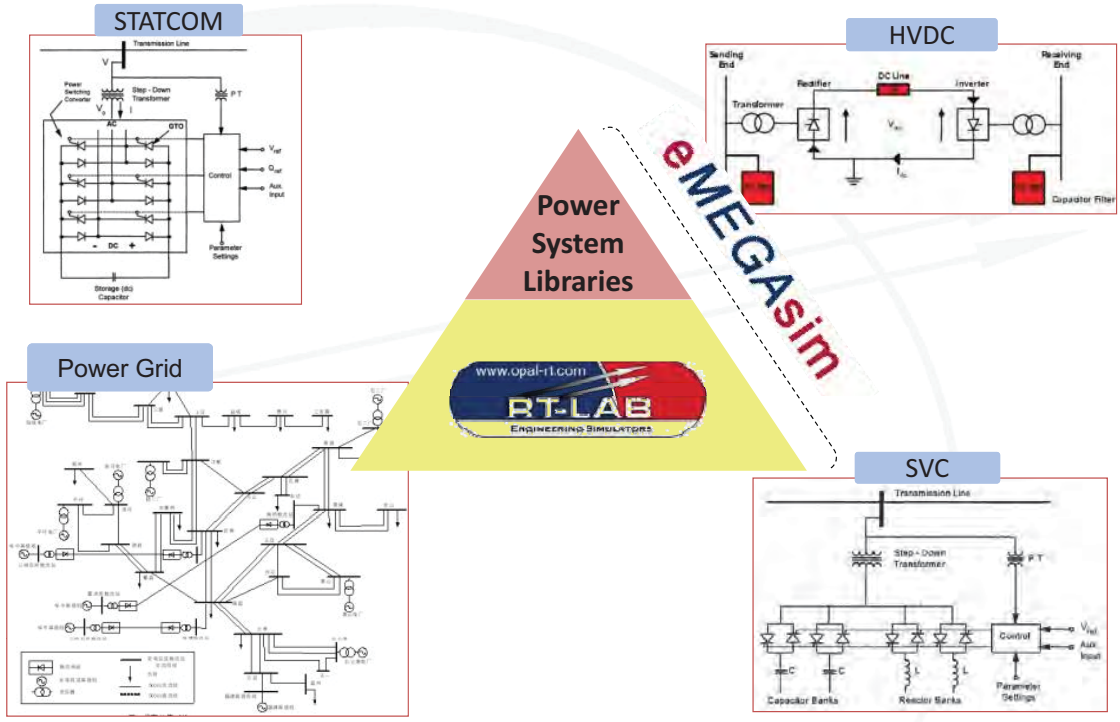
Opal-RT Products



eDRIVEsim : Motor Drive RT Simulator



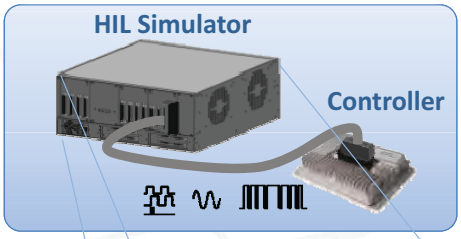
eMEGAsim : Power System RT Simulator

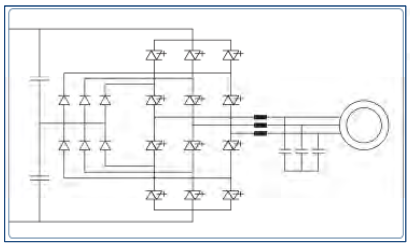


Applications Versus RT-LAB Real-Time Simulators

Hardware-In-the-Loop Simulation

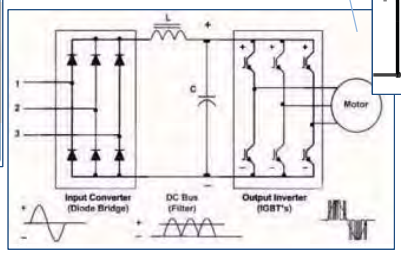
- Hardware In-the-Loop Simulation (HILS)
  - Real-time simulator is connected to actual hardware
- Electric Motor HILS
  - Hardware in the loop with electric motor drive simulated on the HILS, and connected to actual/prototype controller

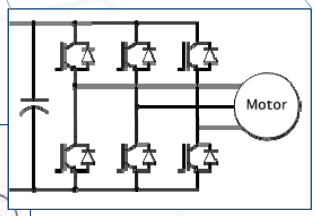




Multi-Level Motor Drive

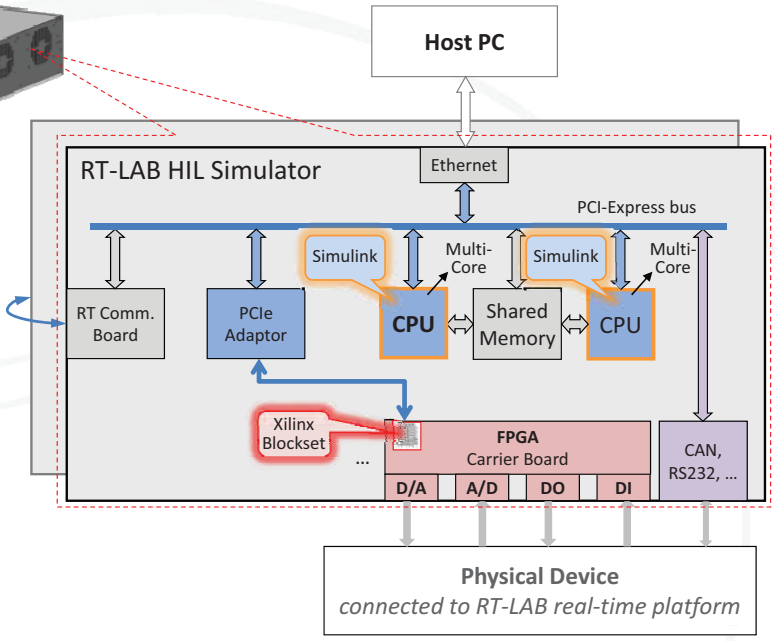
Industrial Motor Drive





PMSM Motor Drive

RT-LAB HIL Simulator



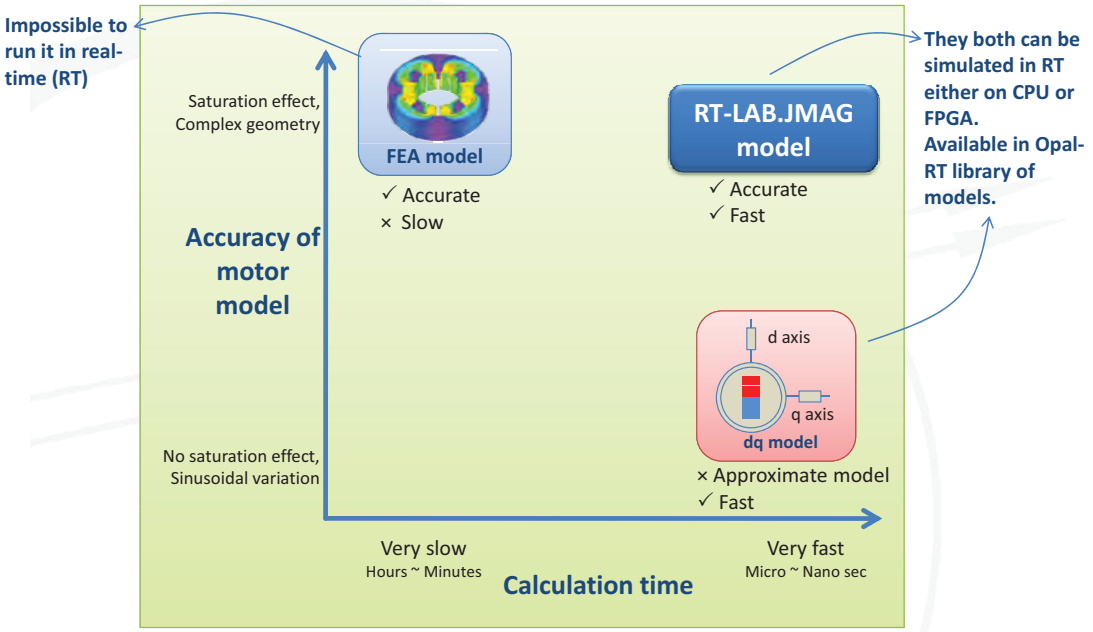
RT-LAB HIL Simulator - Features

- PC- & FPGA-based, multi-processor, multi-core
- Simulink model-based design
- Inputs/Outputs:
  - Ultra-fast FPGA-based I/Os
  - Digital, analog, PWM, encoders, resolvers, etc
- Real-Time OS (Real-Time Linux, QNX)
- Very fast sample times:
  - Intel & AMD Processor Target: 5 - 10 µs
  - Xilinx FPGA Target: 0.2 – 2.0 µs (Model update at: 5-20 ns)

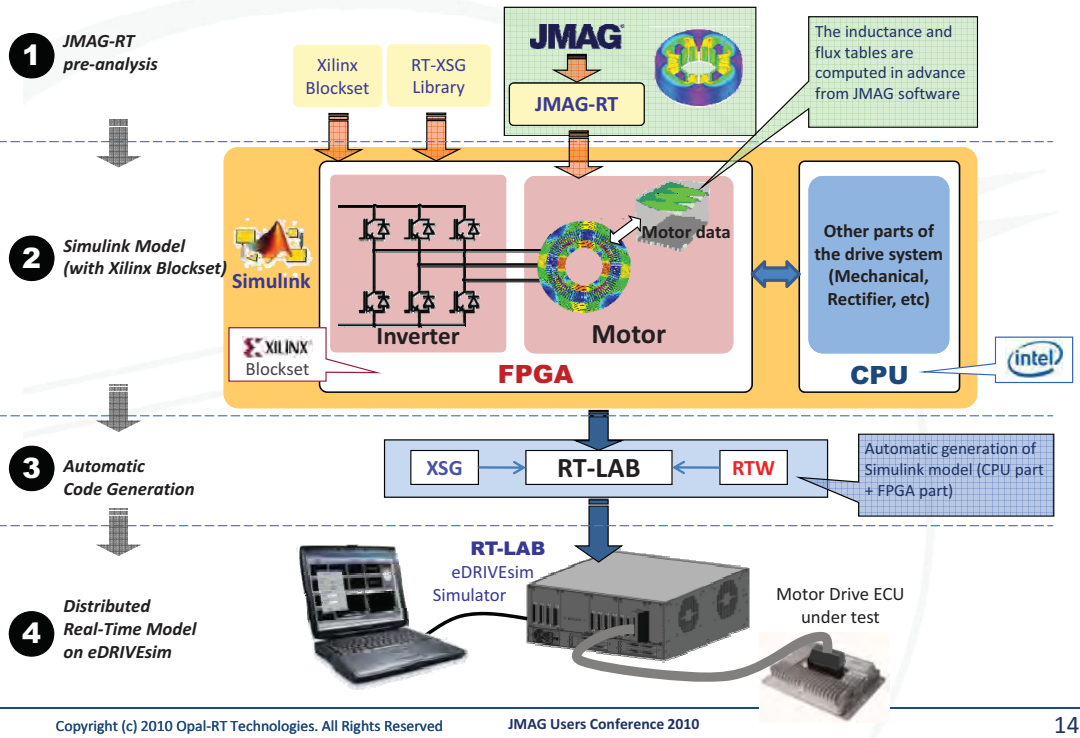
Features

- **Speed:** Very small simulation step down to 0.25 us (FPGA), 8 us (PC processor)
- **Scalability:** Support of complex simulations with modular distributed processing:
  - On multi-processors
  - On multi-cores
  - On multiple FPGA boards
- **Accuracy:**
  - Different types of electric motors (PMSM, BLDC, IM)
  - Inverter dead-time, Regenerative braking
  - Fault conditions and modes
  - Modeling of saturation effects of magnetic material using Finite Element-based model in real-time (from **JMAG-RT**)

FEA-based Simulation compared to formula conventional model

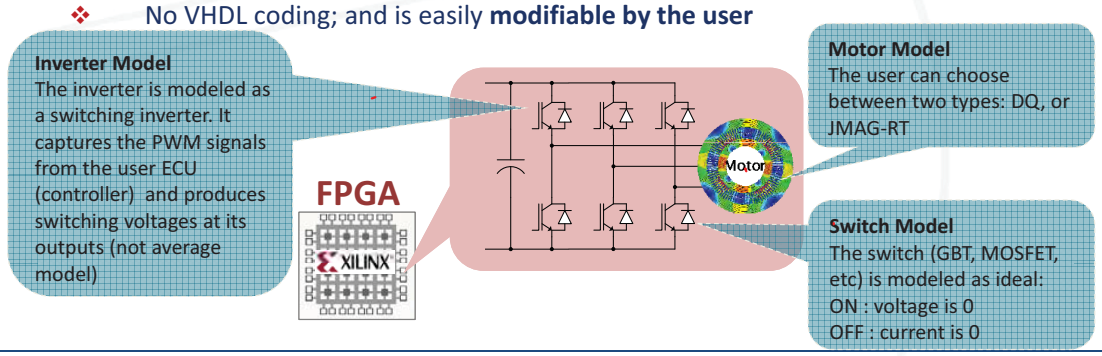


How JMAG-RT is integrated in RT-LAB simulator

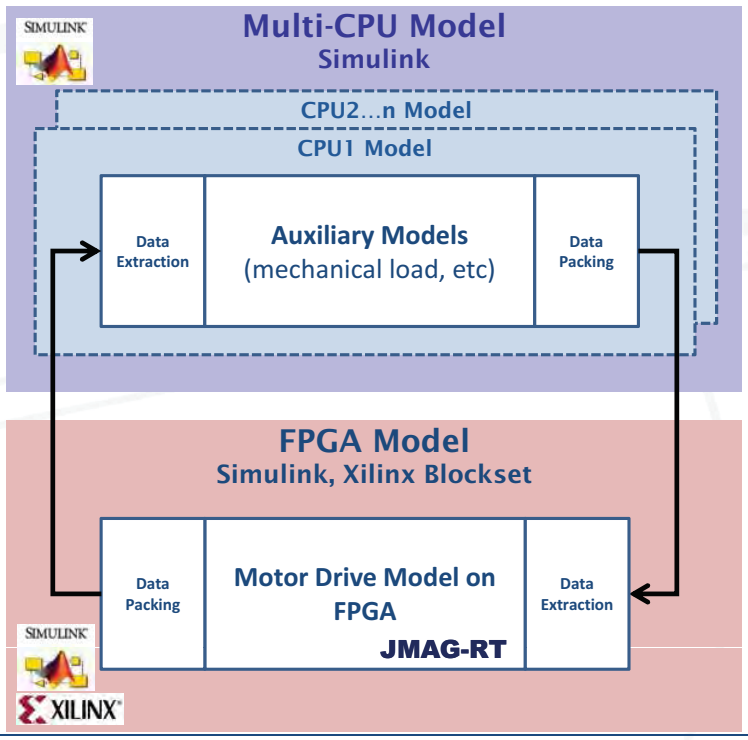


FPGA-Based motor HILS - Description

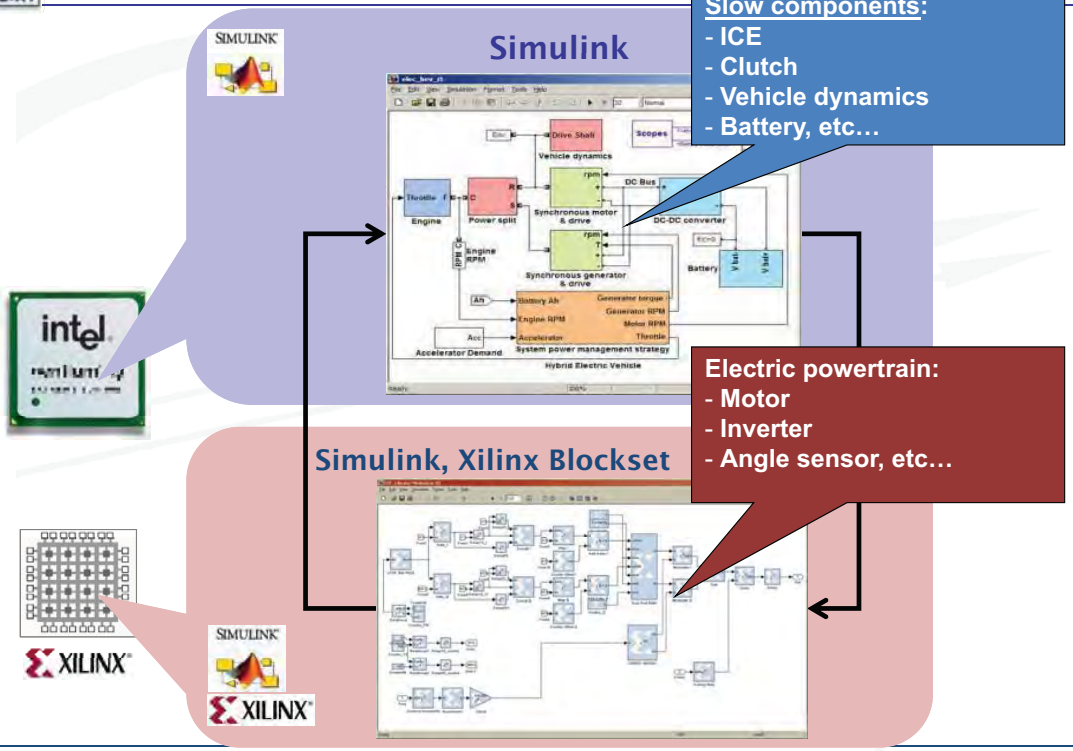
- Complete motor drive:
  - DC link, inverter, motor
  - Internal PWM generator for autonomous testing
  - PWM input capture and analog outputs
  - Different angle sensors emulated: Incremental, Resolver, Hall effect
  - Mechanical load can be easily added on CPU
- Motor model is based on **JMAG-RT®**
- Implemented on powerful Virtex 6 FPGA (also Virtex 2, and Virtex 5)
- Completely designed in Simulink® and **Xilinx® Blockset**
- No VHDL coding; and is easily **modifiable by the user**



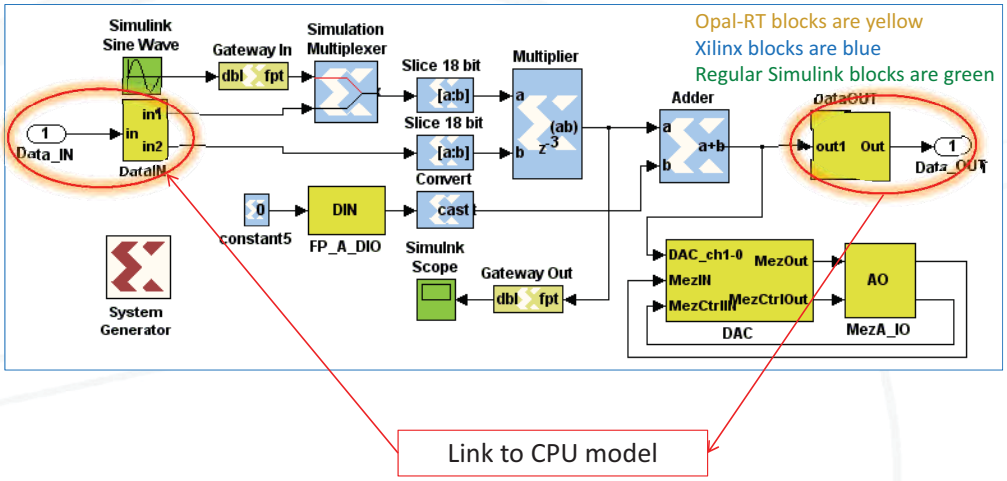
Model Structure in RT-LAB



Example Model - HEV

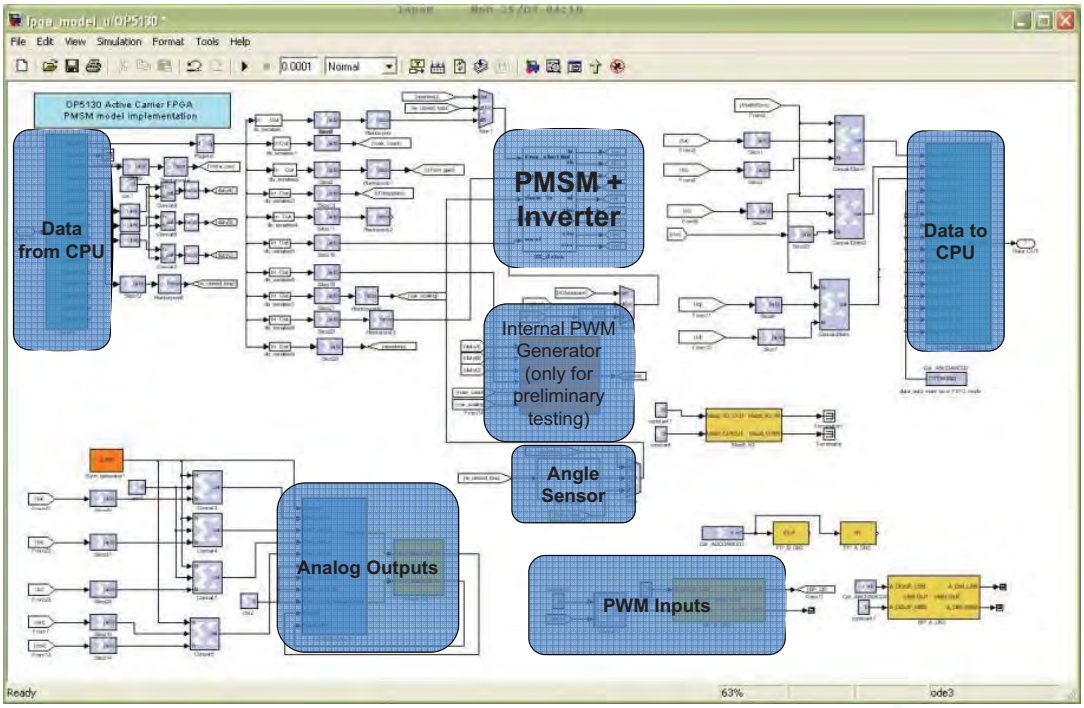


Typical Simulink Model for FPGA on RT-LAB

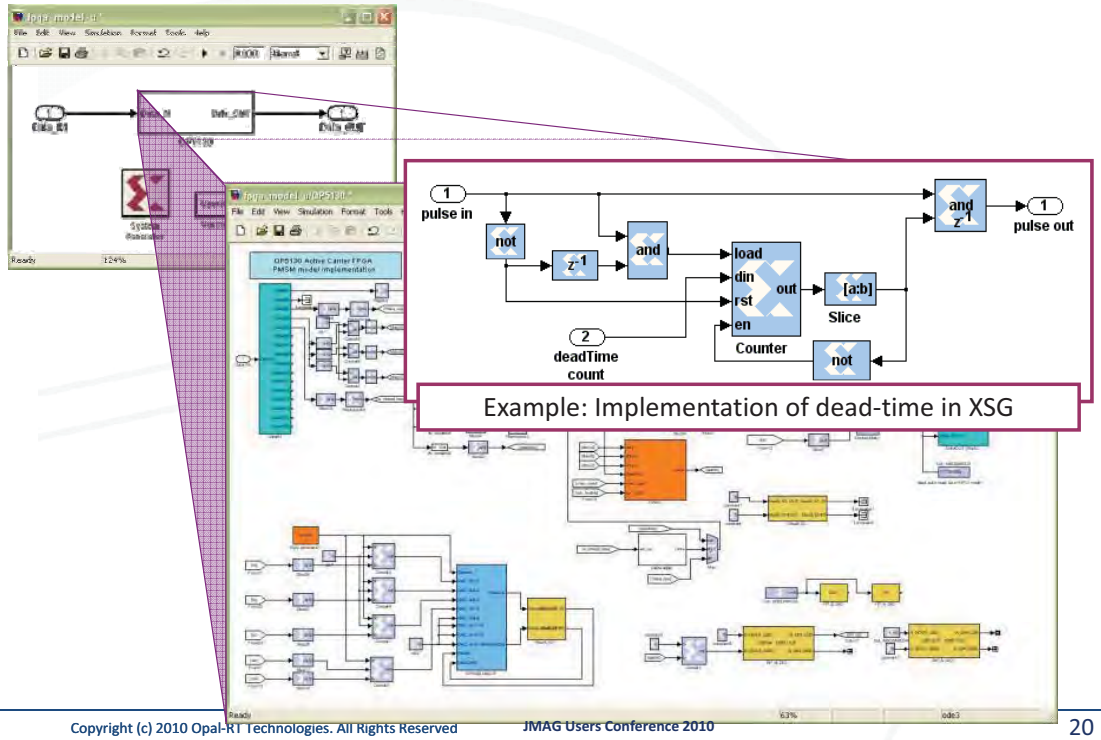


The example model:
- multiplies two numbers coming from another subsystem (DataIN)
- adds a number coming directly from the digital input block (DIN)
- the result is sent to the analog output (DAC-AO)
- and sent to other RT-LAB subsystems (DataOUT)

Modeling for FPGA from within Simulink – PMSM Drive



Modeling for FPGA from within Simulink – Dead Time Example



Example: Implementation of dead-time in XSG

Motor Drive Library for FPGA

- Opal-RT delivers a library of advanced motor drive models.
- This library of FPGA models contains :
  - PMSM machine
  - BLDC machine
  - JMAG-based PMSM model
  - 3-phase inverter model
  - Internal PWM modulator with dead-time
  - Resolver encoder, resolver-to-digital decoder
  - Quadrature encoder
  - Hall effect sensor

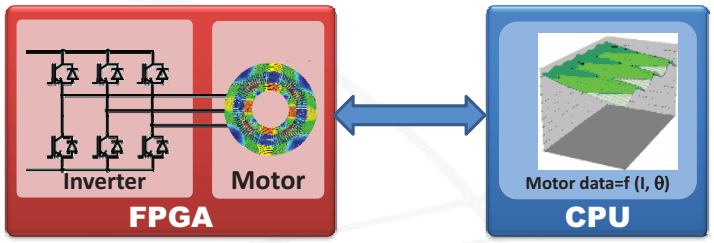
Latest Advancements in Motor Hardware-In-the-Loop Simulation (HILS) based on RT-LAB & JMAG-RT

B. LATEST ADVANCEMENTS

FPGA-Based Simulation with JMAG-RT and RT-LAB

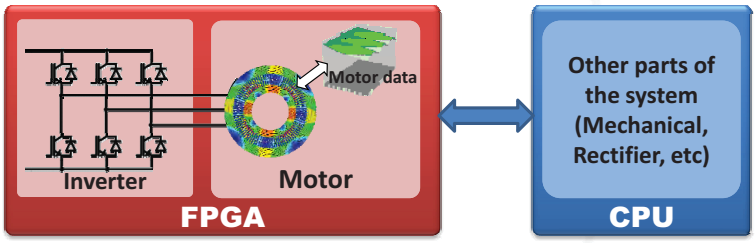
Previously (2005+)

- FPGA:
  - FPGA Virtex 2 Pro
- Model:
  - Motor data on CPU
  - Motor model on FPGA
  - Motor data sent to FPGA
  - Data interpolated on FPGA



Latest Advancement (2009/2010)

- FPGA:
  - Virtex 5
  - Virtex 6
- Model:
  - Complete motor (model + RTT data) on FPGA
  - Room for additional circuitry & functions on the FPGA
  - Option to simulate two motor drives on FPGA



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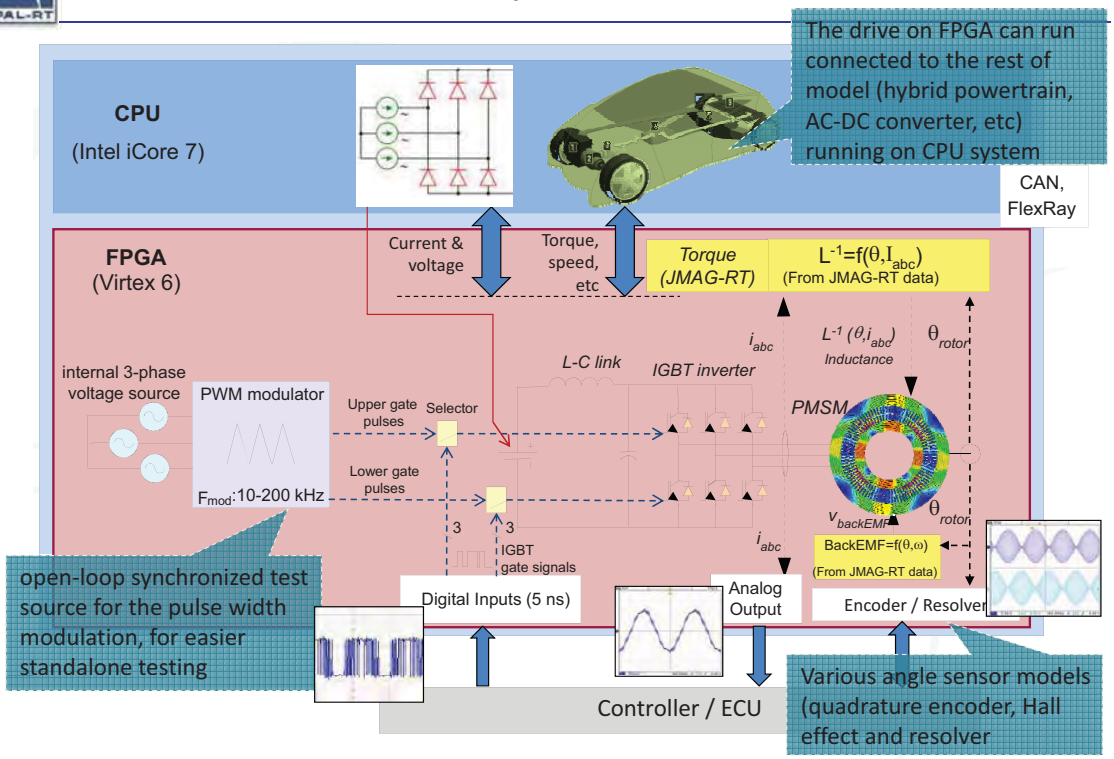
RT-LAB FEA-based PMSM Drive implementation on Virtex-6 FPGA



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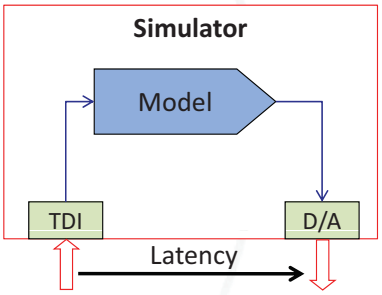
Motor Simulator Timings & Latency

- Timing - The PMSM drive model :
  - runs with an equivalent **5 nanosecond** time step (200 MHz Virtex-6 FPGA card)
  - has an update of **200 - 300 nanoseconds** (PMSM machine DC-link and inverter)
  - The motor drive is directly connected to digital inputs and analog outputs with 1 microsecond settling time on the FPGA card and has a resulting total hardware-in-the-loop latency of **1.2 - 1.5 microseconds**

- Total Delay "from Timed Digital Inputs to Analog Outputs"
- Motor drive HILS: "from Gate Signal Inputs to Current Outputs"
- Latency (maximum values)
  - CPU Target → 2.Ts – 3.Ts
  - FPGA Target → 1.2 – 1.3 µs
    (Ts : Time Step)



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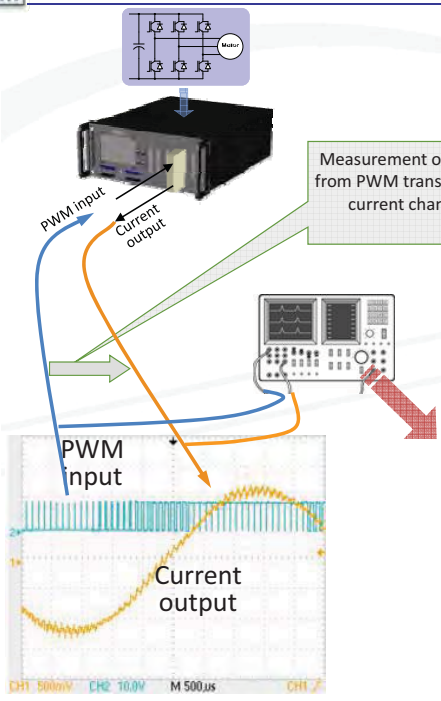
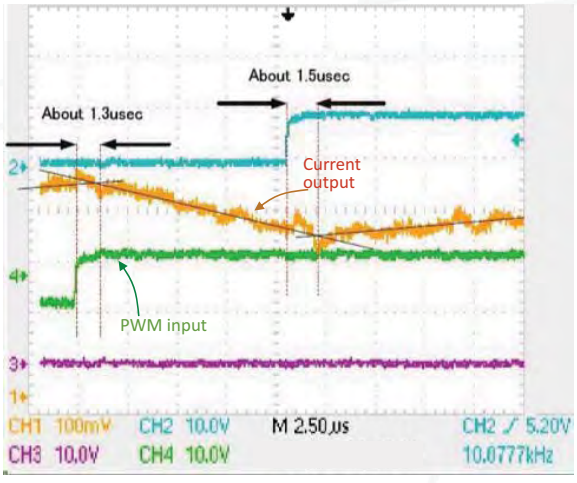
Total Latency Measurement



Delay : «PWM in–to–Current out» (1.3-1.5 us)



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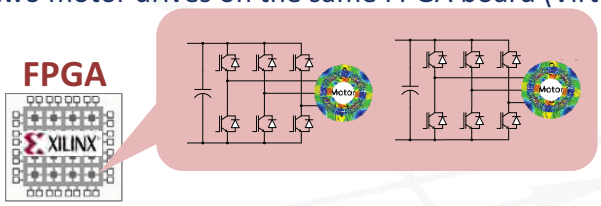
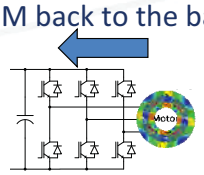
Additional Features and Modes in RT-LAB HILS

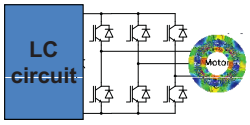
- The HIL simulation of two motor drives on the same FPGA board (Virtex 6) is supported



- Regenerative breaking is supported (when electric braking energy is sent back from the PMSM back to the battery through the inverter)

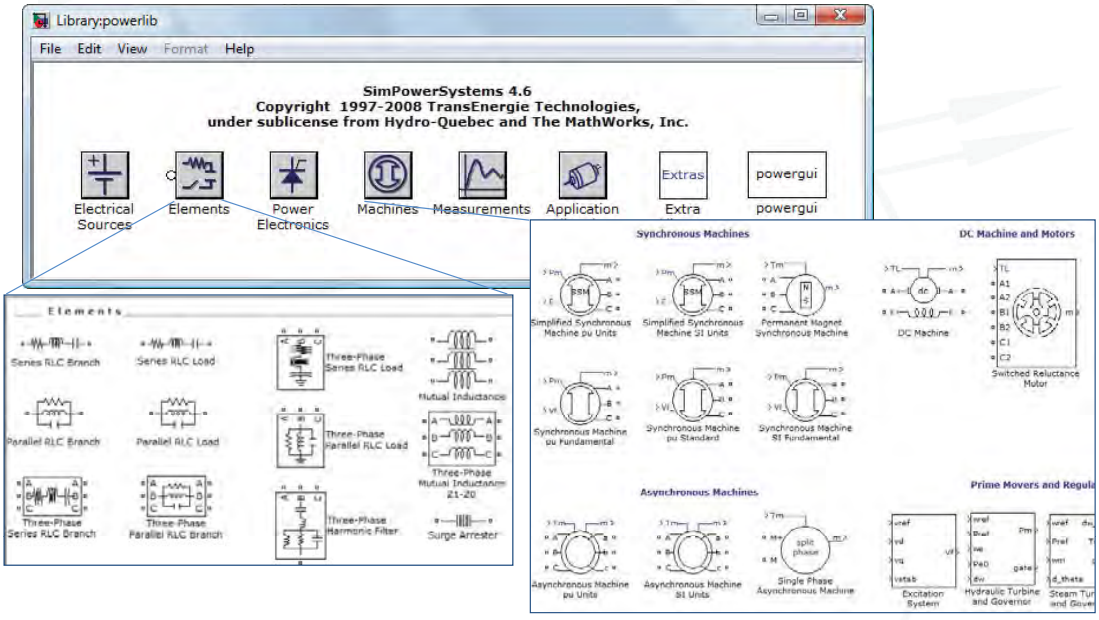


- The DC link in front of the inverter can be modeled with its Inductance and capacitance equivalent circuit



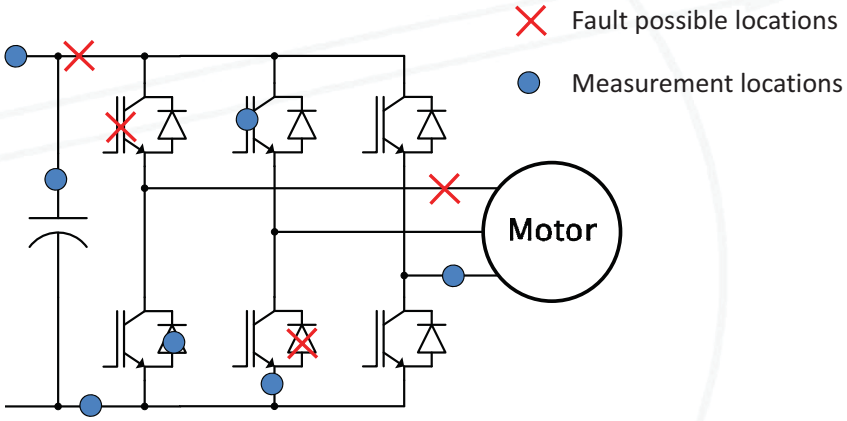
Additional Features in RT-LAB HILS → SimPowerSystems

- Optional Interface with SimPowerSystem
(Special solver developed by Opal-RT for real-time)

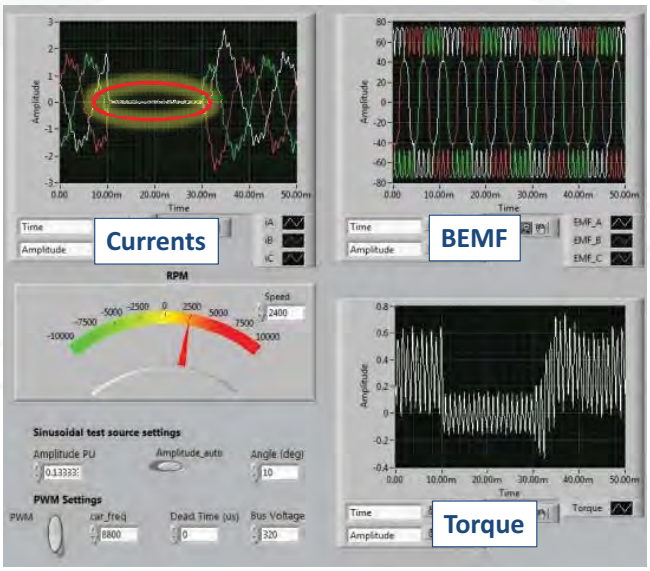


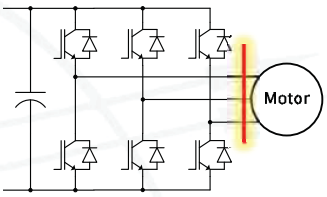
Fault modes

- The PMSM drive model support all these types of faults:
  - IGBT open/short-circuit
  - Diode open/short-circuit
  - Motor stator short-circuits (phase-GND, phase-phase)
  - DC-link short-circuit

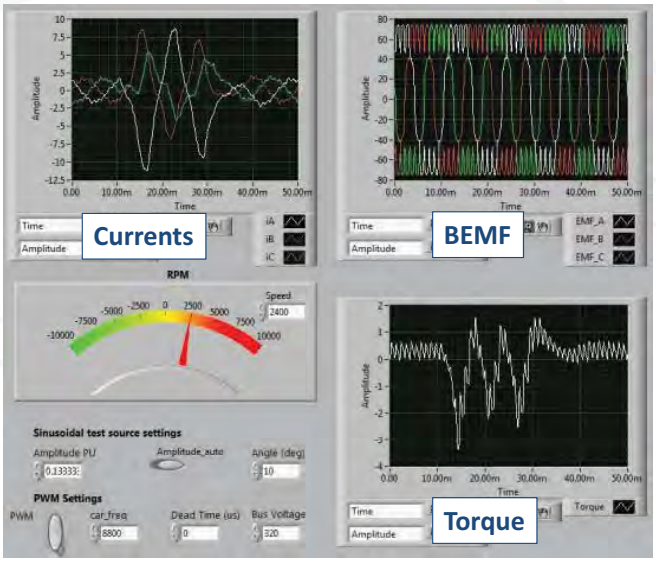


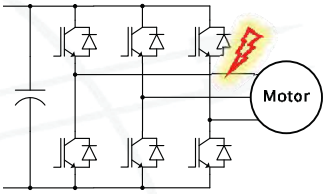
Example: Open Stator Test





Example: Phase to Ground Short Circuit



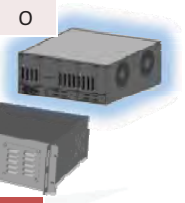


Simulator Chassis

Legend	
O	High
Δ	Medium
	Low

OP5600

Size	Power	I/O
O	O	O



Wanda 4

Size	Power	I/O
Δ	O	O

Test Drive

Size	Power	I/O
		O

Wanda 3

Size	Power	I/O
Δ	O	Δ

PC104

Size	Power	I/O
O		Δ

HILBox

Size	Power	I/O
	O	O

MX Station

Size	Power	I/O
O	Δ	Δ

Power	Processing power
Size	Chassis size
I/O	Number of I/O lines

Year

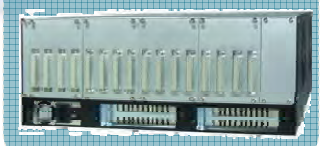
New HILS platform: OP5600

High-Performance and Open Hardware System
- Multi-Core INTEL processor
- 4 or 5 cores up to 3.3 GHz
- PCI Express, 7 µs model step
- Real-time LINUX or QNX

Two FPGA Options
- SPARTAN3 for Fixed-point models
- Virtex 6 for floating-point large models

Large VIRTEX-6 FPGA with on-board memory
- Can simulate two JMAG Motor models
- 160 -200 ns model step
- 1.3 µs from gate pulse to motor current output
- Floating point powerful solvers
- User programmable (option)

Back-end I/O Connectors

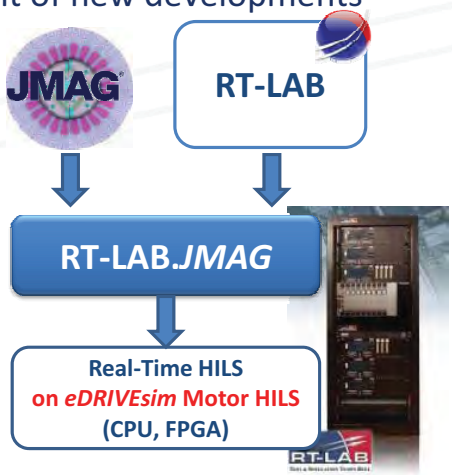


Configurable I/O directly controlled by FPGA
- Up to 96 fast analog I/O, 500 ns, 1 µs or 2.5 µs
- Up to 192 fast discrete IO, 5V to 30V, <100 ns
- Integrated analog signal conditioning

Front-end I/O signal monitoring with mini BNC connectors

Conclusions

- The combination of RT-LAB & JMAG-RT gives the user the most advanced motor HILS
- JSOL and Opal-RT are pioneers in answering the needs of the motor drive design and testing by continuously being at the forefront of new developments



Thank you !

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- The Mathworks (http://www.mathworks.com/)
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