# The State-of-the-Art in Hardware-in-the-Loop Simulation of Motor Drives

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Abstract :
Hardware-In-the-Loop simulation (HILS) is an integral part of the design and testing process of electric motor drives and of systems incorporating variable speed drives. And OPAL-RT has been a pioneer in teaming-up with JSOL to provide the most advanced HILS system to motor control and system engineers, to help them conduct an ever increasing number of tests, before field-testing and deploying the final product.
In last year's JMAG Users Conference, OPAL-RT presented the current state of Motor HILS based on JMAG-RT and the FPGA platform, and described the hardware and modeling development that was taking place. In this year's JMAG Users Conference, we present the state-of-the-art in Motor HILS, including multiple motors and inverters, all simulated on FPGA, in normal, faulty, and rectification modes, and with motor models based on JMAG-RT software.
Key features of the new advanced drive models is its ability to simulate DC filter circuits on the FPGA as well as simulating faults on several location including inverter IGBTs and DC filter components faults as well as faults on motor terminals. Those features demonstrated with a real-life test case, require the implementation of a low-latency floating point electrical circuit solver on a powerful Virtex 6 FPGA chips.

There are no presentation materials included.