Leveraging JMAG-RT and FEA-based Models for High Fidelity Real-Time Test in FPGA

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Abstract :

Real-time test in the area of power electronics provides unique challenges that are difficult to address with traditional hardware-in-the-loop (HIL) systems. The high speed discrete switching states of power electronics systems mean that the simulation system needs to run on the order of 1 us to provide useful numerical results, and the benefits during algorithm development are directly related to the fidelity of the model. A good test system allows a control engineer to speed up the design cycle by allowing control testing to start without physical hardware, to test novel control algorithms without endangering hardware and to see potentially un-measureable parameters within the system. To address these issues and to provide a platform for HIL testing of electric motor systems, National Instruments has partnered with JSOL Corporation and developed field programmable gate array (FPGA) models that use JMAG-RT as a means to deploy the high-fidelity of an FEA simulation into the high speed of a FPGA processing node.

Leveraging JMAG-RT and FEA-based Models for High Fidelity Real-Time Test in FPGA

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System Engineer
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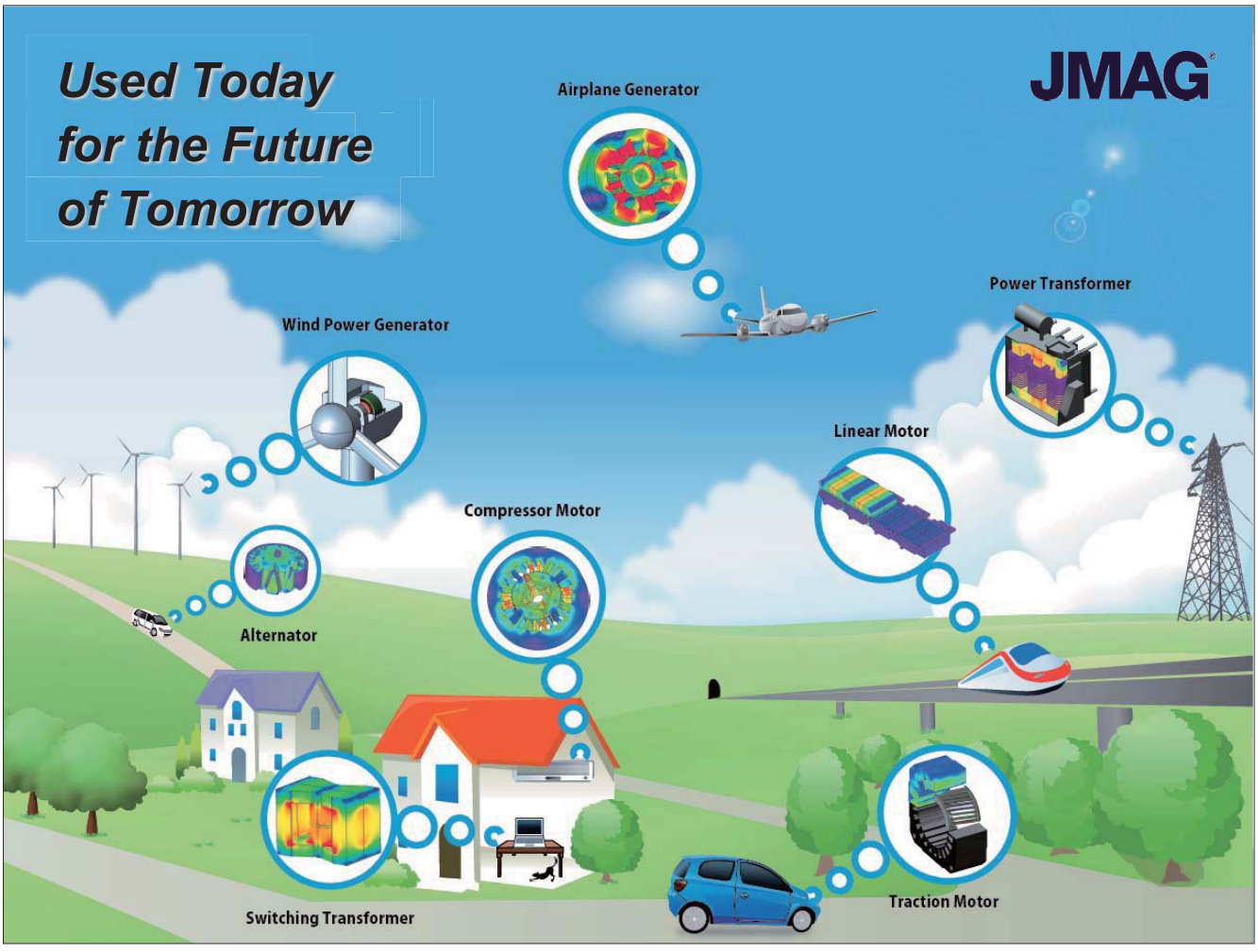

Electric Motor Presence

Automotive

Energy

Off-Highway

Aerospace

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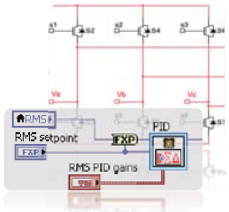
NI Vision for Power Electronics

Graphical Co-Simulation (Multisim, LabVIEW FPGA)



Design

Physical Testing

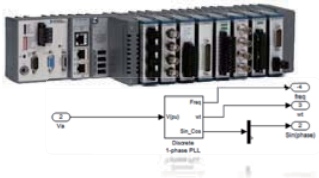
Prototyping

HIL Validation

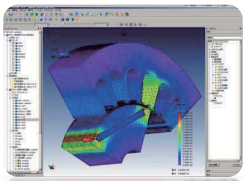
Deployment

Power Electronics Testing (Bloomy Energy, PXI)

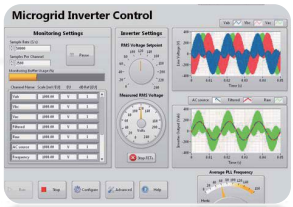
Rapid Control Prototyping (Multicore CompactRIO, SIT)



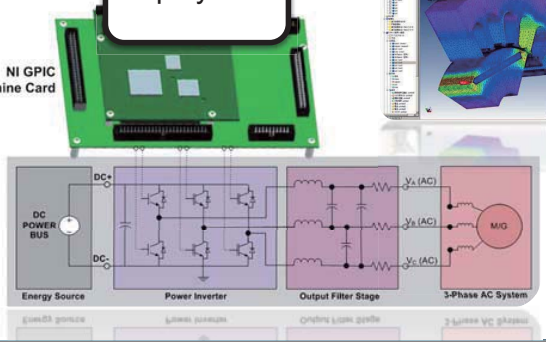
Real-Time HIL Simulation (JMAG, KGC, SET, FlexRIO, VeriStand)



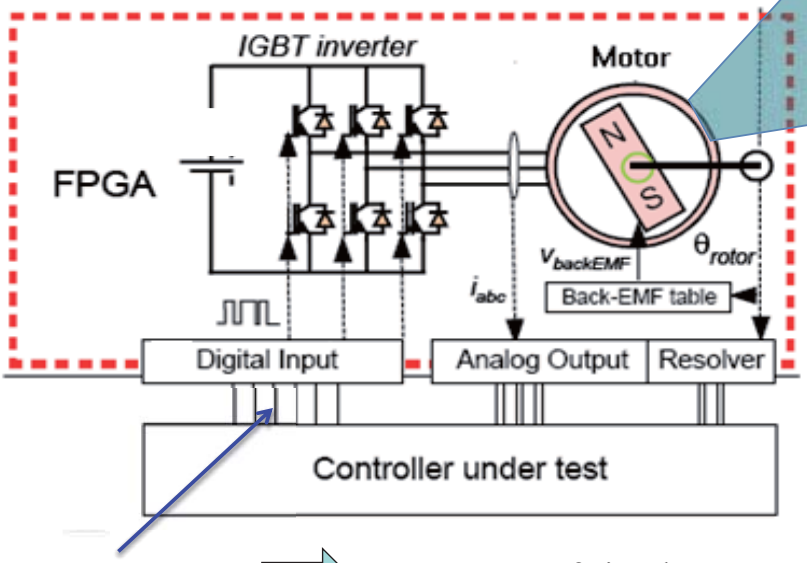
Commercial Deployment (General Purpose Inverter Controller)



NI GPIC Mezzanine Card



Electric Motor Systems



25kHz PWM ⇨ Loop rate of simulator > 250k

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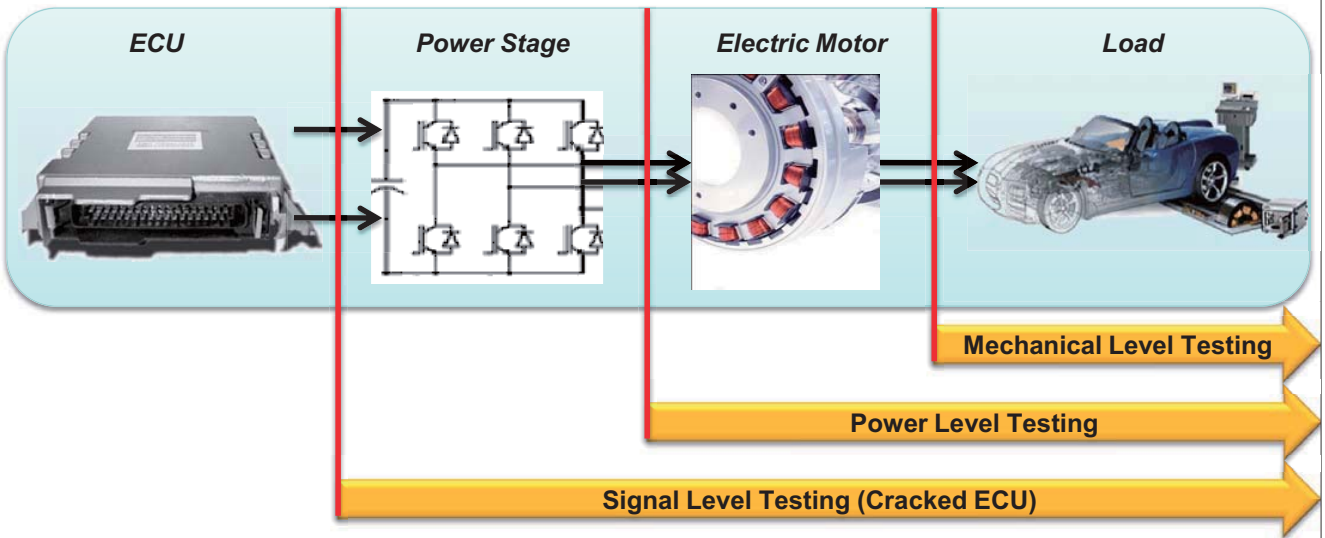
Electric Motor Testing: Traction ECU



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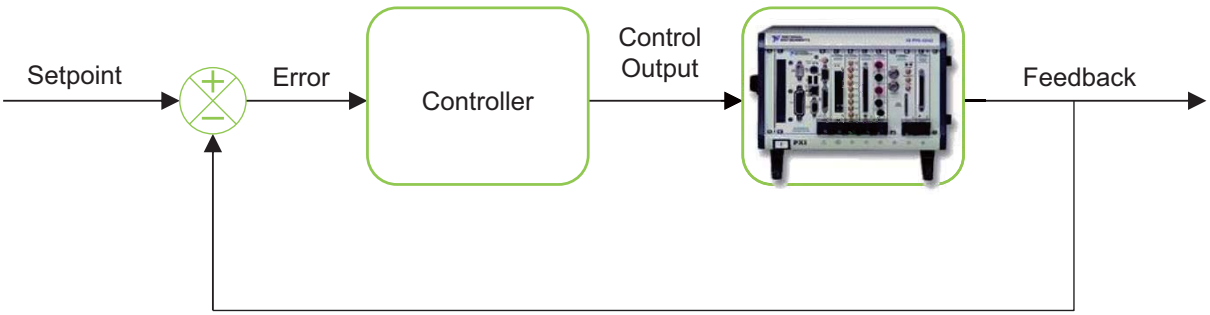
Why is HIL important?

- Parallel controller development
- Decreased controller tuning time
- Protection of expensive prototype motors
- Ability to safely complete potentially destructive tests

HIL Simulation for Power Electronics



Keys to success for power electronics simulations

- High fidelity models
  - Non-linear
  - Time varying
- Sub 1us timing
- High speed I/O (1-10x the loop rate)

FPGA-Based Power Electronics HIL

JMAG®
Simulation Technology for Electromechanical Design

SET

NATIONAL INSTRUMENTS™

MAC SYSTEMS

KGC

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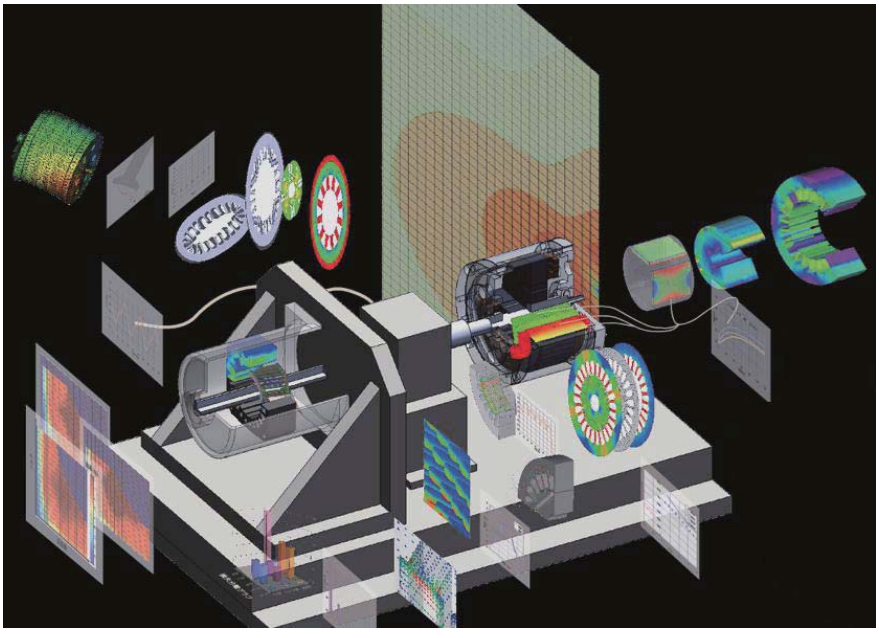
JMAG RT Add-Ons for LabVIEW and NI VeriStand



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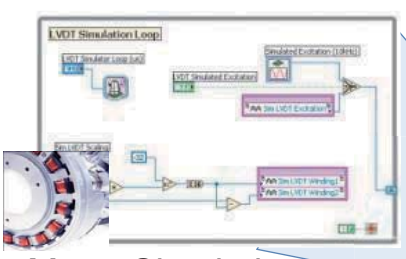
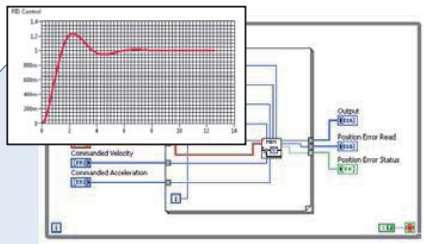
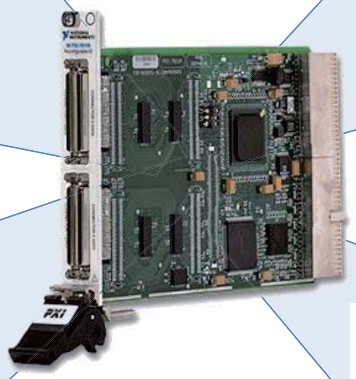
FPGA-Based I/O Interfaces

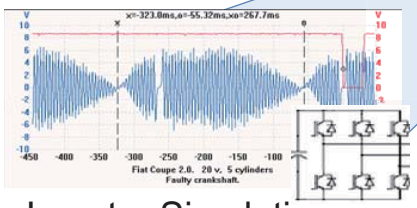


Motor Simulation

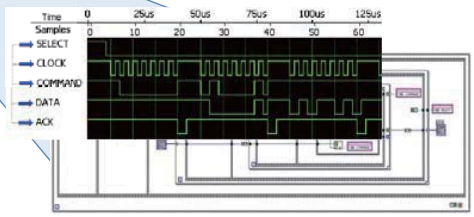


High-Speed Control





Inverter Simulation



Custom Protocols

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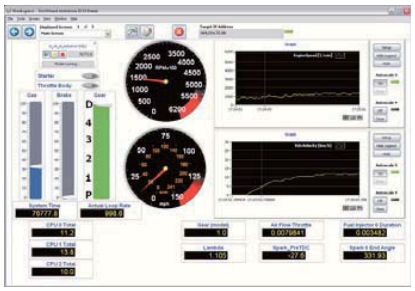
NI Real-Time Testing Platform

Real-Time Processor



NI VeriStand

Fault Insertion

FPGA Based I/O

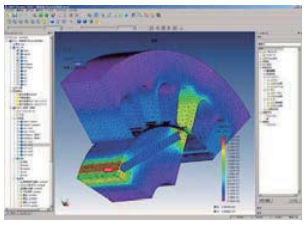
Bus Interfaces

NI PXI Platform

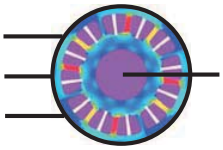
Analog/ Digital I/O

Instrument Grade and RF I/O

JMAG High Fidelity Simulation



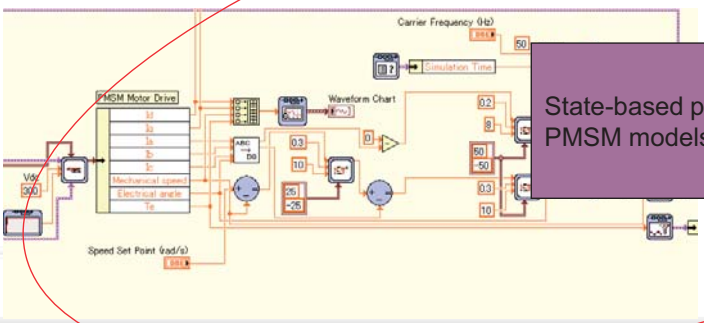
JMAG FEA



JMAG-RT model
·RTT file; look-up table
·Binary

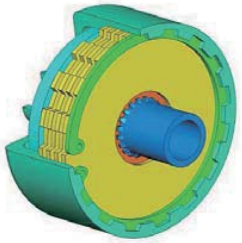
NI Real-Time Hardware

Converter
•Reads RTT file
•Generates LUTs



State-based parameters for PMSM models

Creating High Fidelity Models

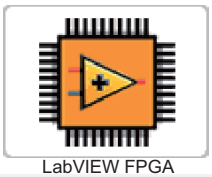


NI VeriStand
Real-Time Test
Software

JMAG Add-On for NI VeriStand

Windows PC

LabVIEW Real-Time



LabVIEW FPGA

Model	Execution Target	Simulation Fidelity	Real-Time Simulation Speed
FEA with JMAG	Windows	High	Non-RT: Minutes to hours
DQ Model with Constant Parameters	Real-Time	Low	20-30 us
	NI FPGA	Medium	1-2 us
DQ Model with JMAG-RT	Windows Real-Time	Medium	20-30 us
	NI FPGA	Medium	2-3 us
JMAG Spatial Harmonic Model	Windows Real-Time	Medium	20-30 us
	NI FPGA Hardware	High	~1 us

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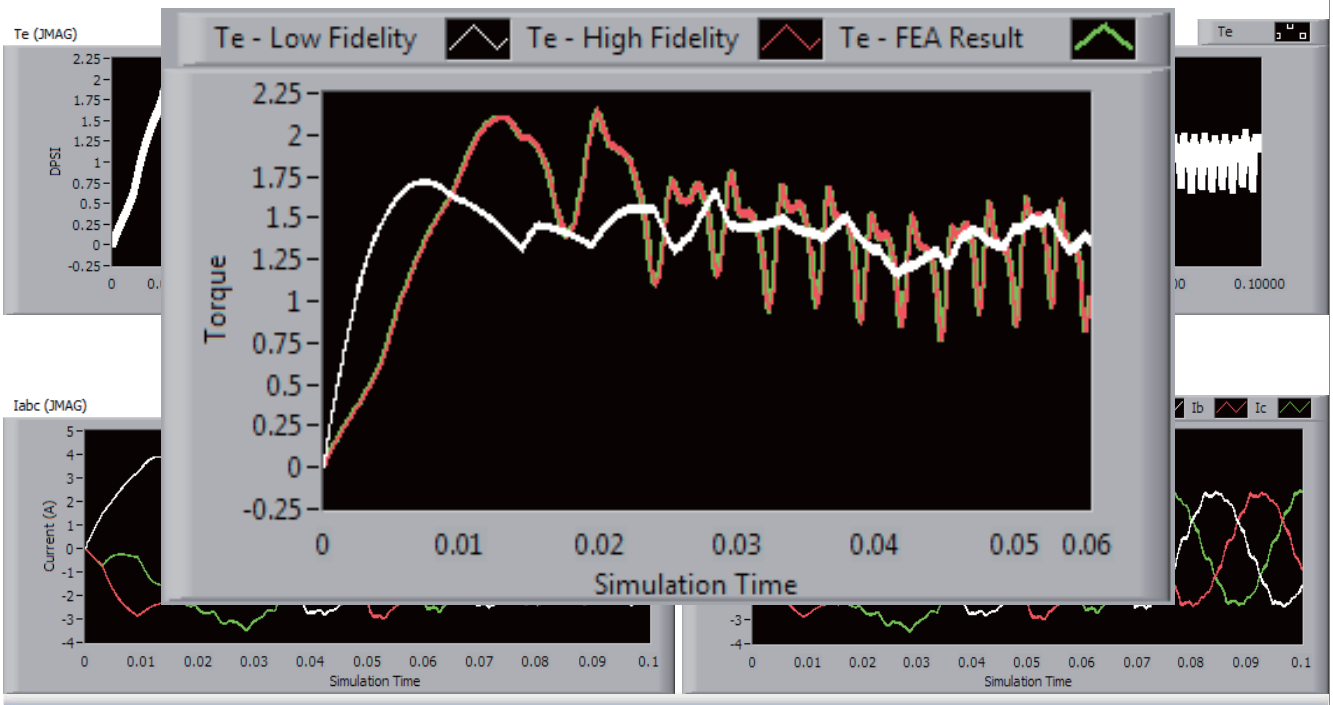
JMAG-RT Versus FPGA



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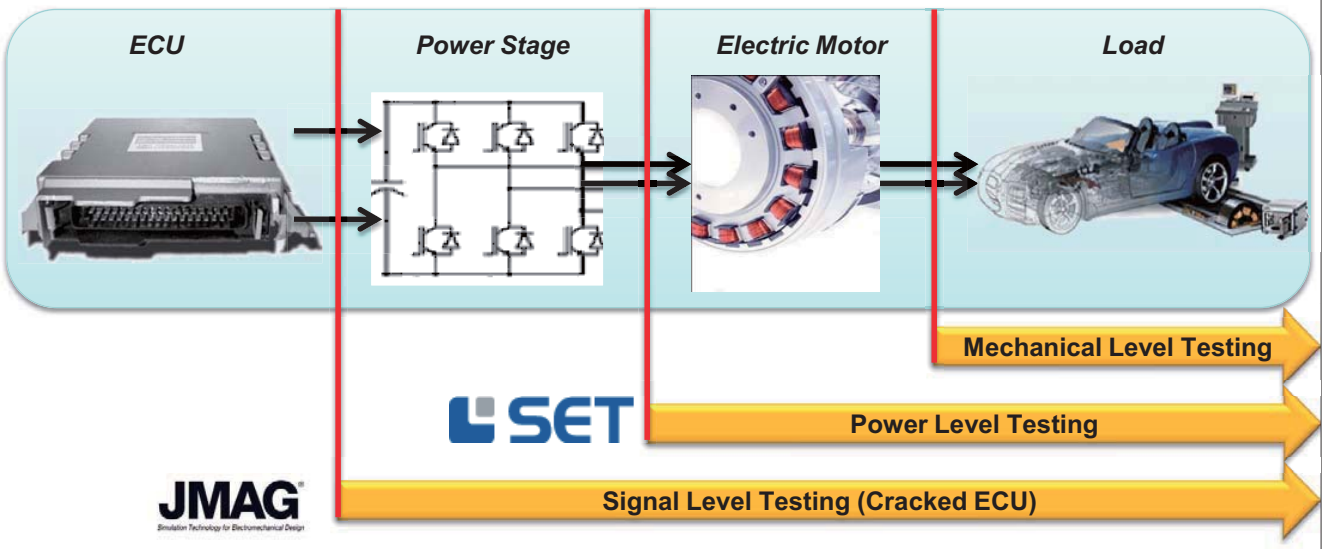
Electric Motor Emulation



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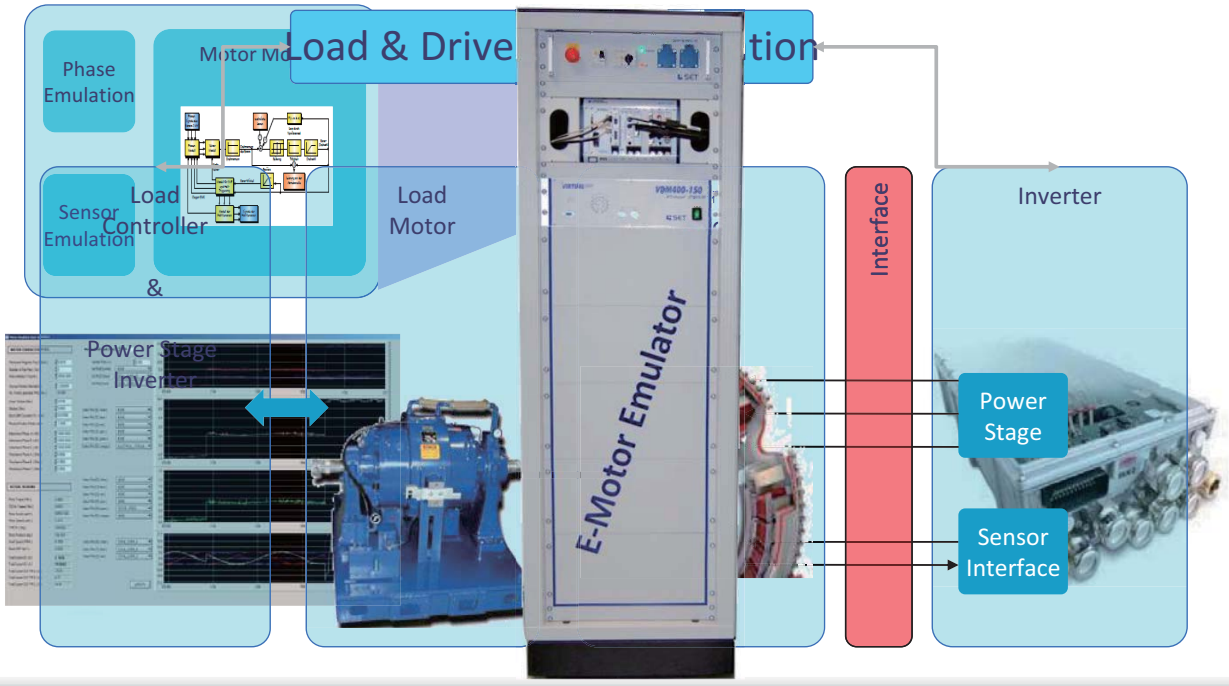
EME



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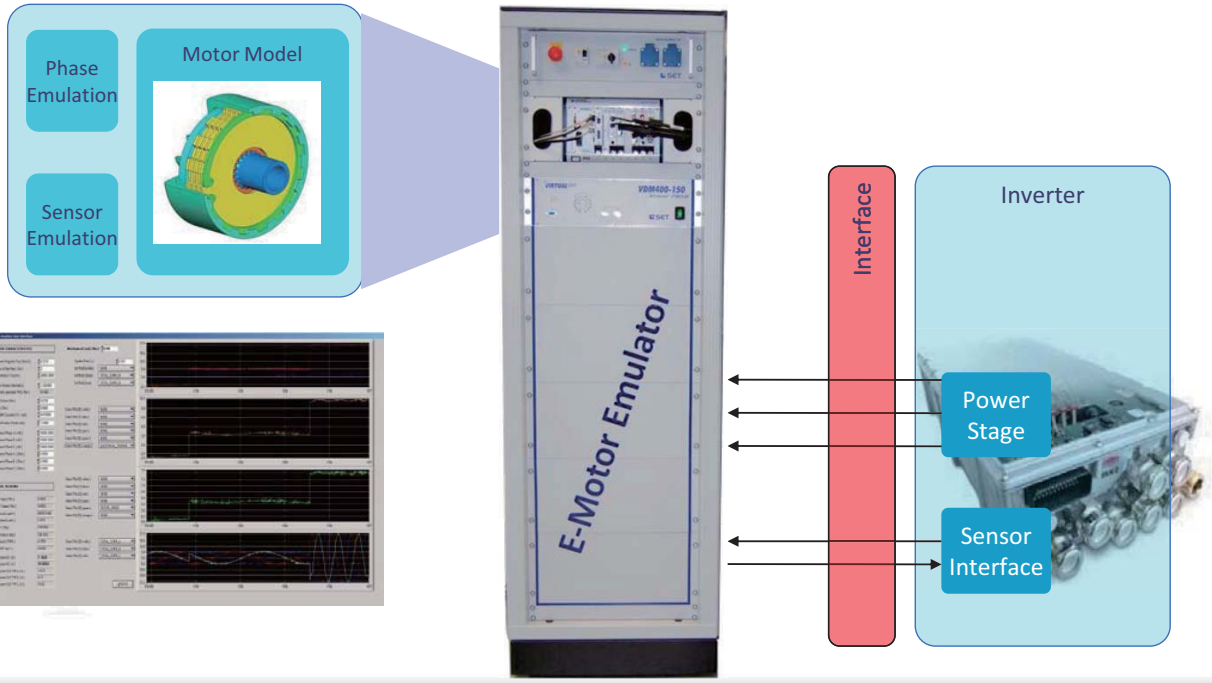
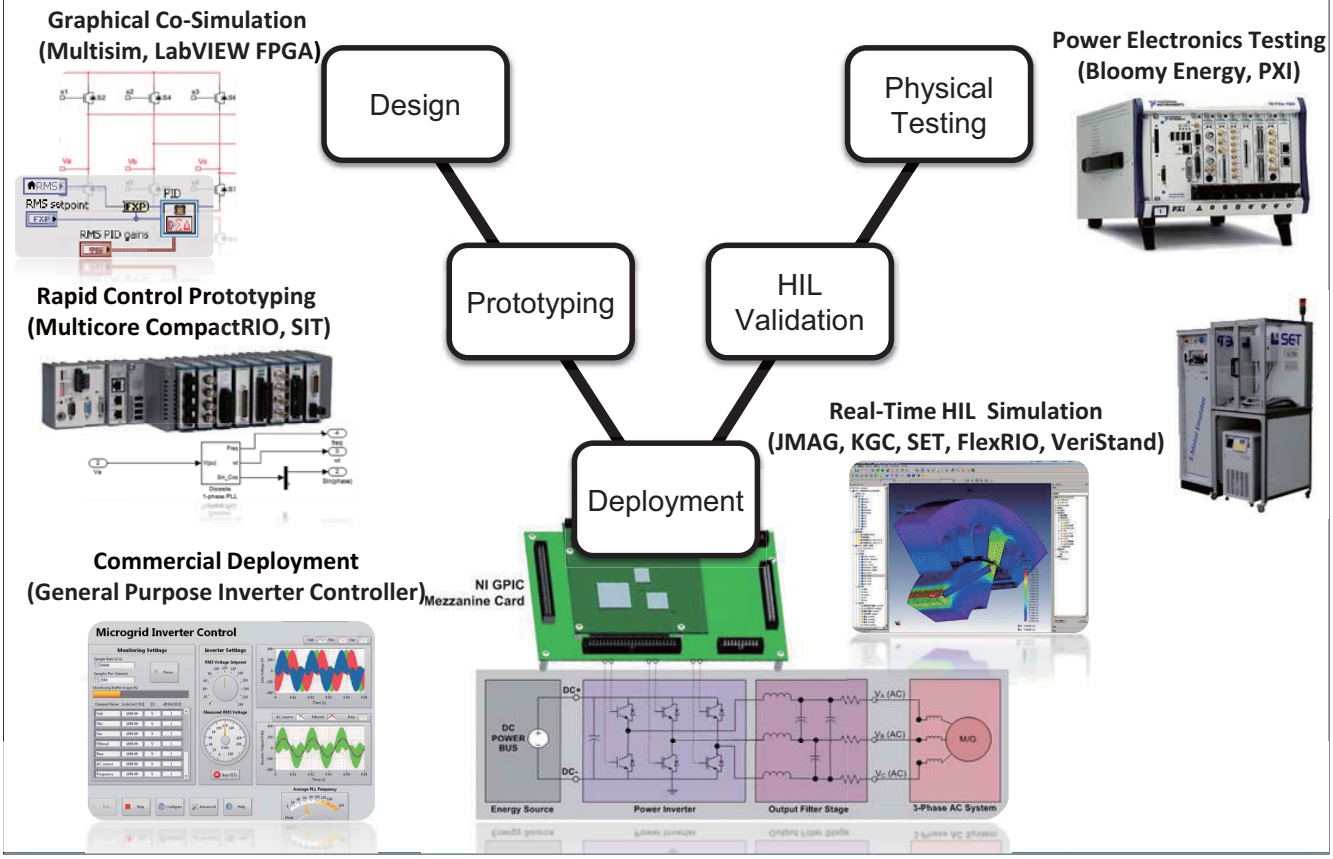
EME



NI Vision for Power Electronics



Future Investments

- Further integration with JMAG-RT motor types
- Advanced, non-linear inverter models
  - Importing models from other environments
  - Lookup table-based inverter models
- Variable time step, energy-based inverter model

Summary

- JMAG Add-on For VeriStand and LabVIEW
- Modeling Options
  - Micro-processor based model (20-30 usec)
  - FPGA-based d-q model with constant parameters (<1 usec)
  - FPGA-bsed d-q model with JMAG Addon (~1 usec)
  - FPGA-based Spatial Harmonic Model with JMAG (~1 usec)
- High-Fidelity motor emulation with SET