JMAG in RT-Lab HIL Simulator

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Outline

About us | HIL Solution | Successful stories

OPAL-RT in Brief

- Established in 1997
- RT-LAB: Real-Time Simulation Platform for Simulink™ and SystemBuild™
  - Hardware in the Loop for Demanding Simulations
  - Distributed, Parallel Processing using Off-the-Shelf Technologies – PC, FireWire, QNX, NI, FPGA etc
  - Scalable Power for the most complex dynamic models
  - Comprehensive API for on-line tools for visualization and interaction, eg LabVIEW™
- 80+ Employees
- 60% of turnover reinvested in R&D.
- Over 350+Customers Worldwide…

Core Markets & Main Customers

- Automotive
  - GM, Ford, Toyota, Hyundai, Peugeot, Audi/VW
  - Tier 1: Delphi, Bosch, Visteon, Allison transmission

- Electrical & Power Electronic
  - GE, ABB, Hydro-Quebec, Mistubishi Elecric etc.

- Academic Research & Education
  - US: MIT, Berkeley, Michigan, Ohio state, Texas etc.
  - Canada: Windsor, Waterloo, Alberta, UQ etc.

KeLiang in Brief

- 149 Employees, since 2007.[Founded in 2003, Re-register in 2007]
- 2 Offices (Bejing & Xi'an), HQ:Shanghai,CaoHeJing
- 3 Main Business Division
  - Automotive
  - Power Grid
  - Defense
- 4 Main Engineering Service
  - Virtual Plant simulation
  - Rapid Control Prototyping
  - Hardware In the Loop Test
  - Integrate Validation

Core Markets Main Customers

- 200+ Customers

Outline

Part 1

About us

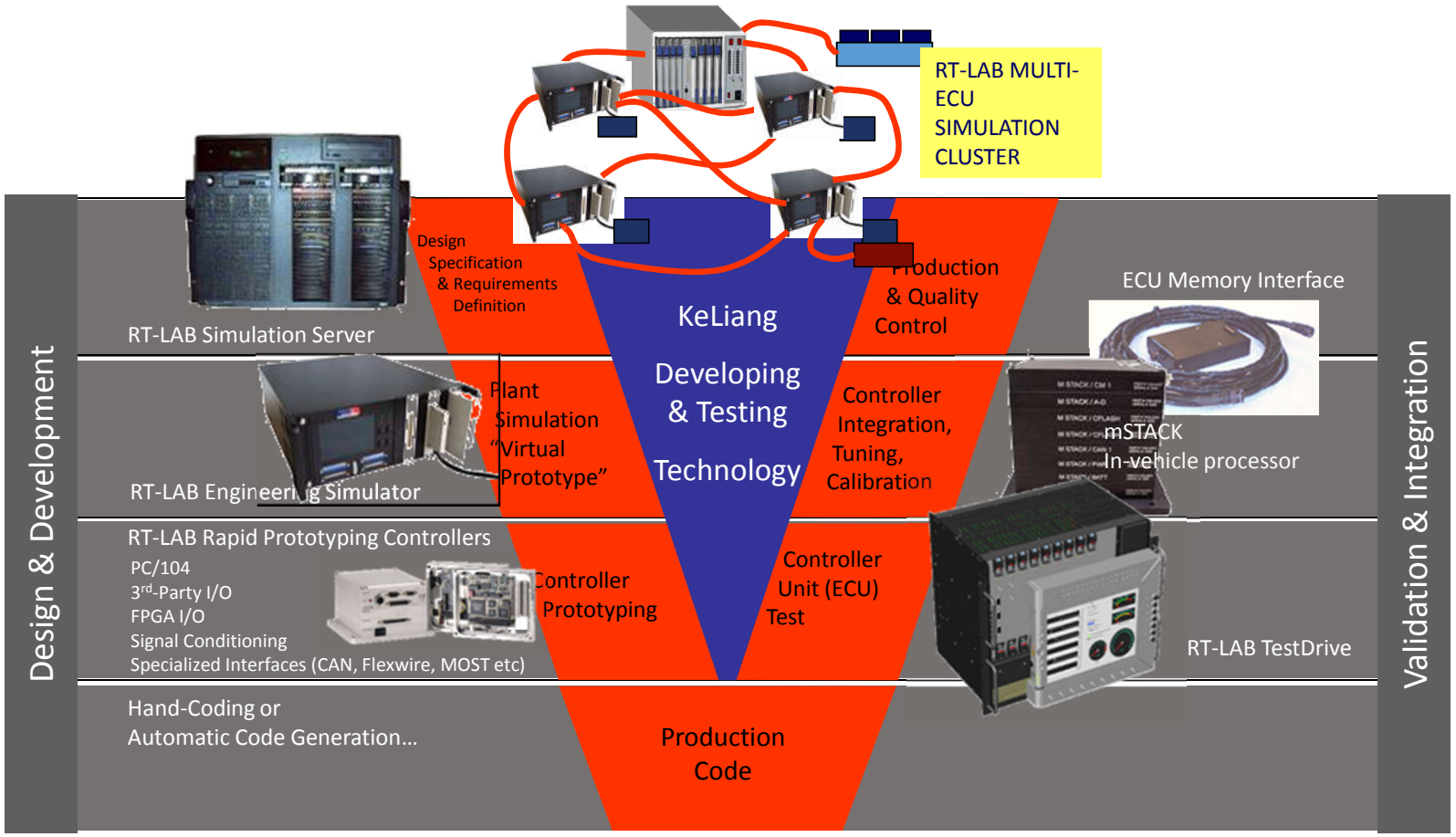
Part 3

Successful stories

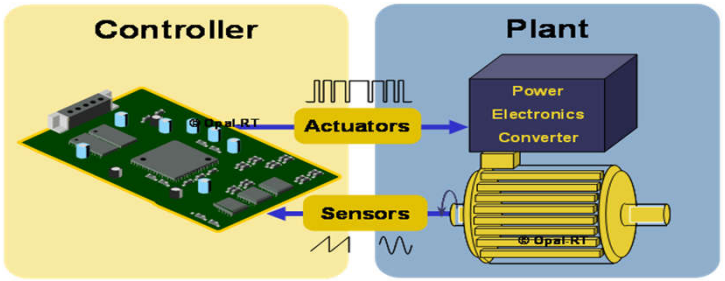
Part 2

HIL Solution

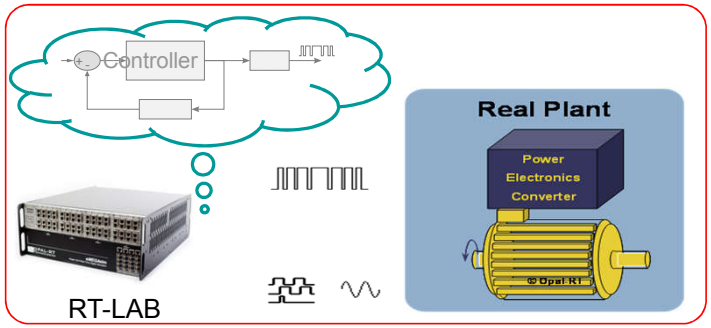
Design Tool Chain



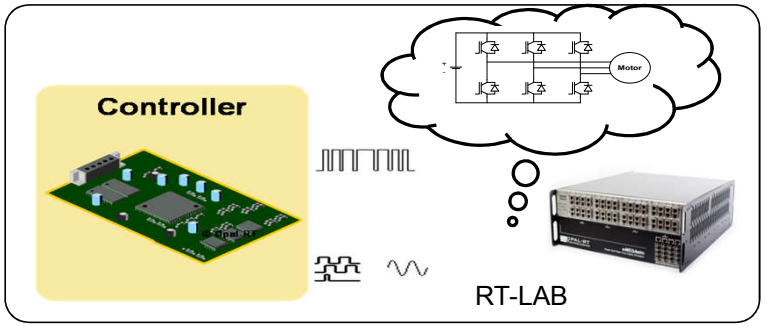
RCP & HIL



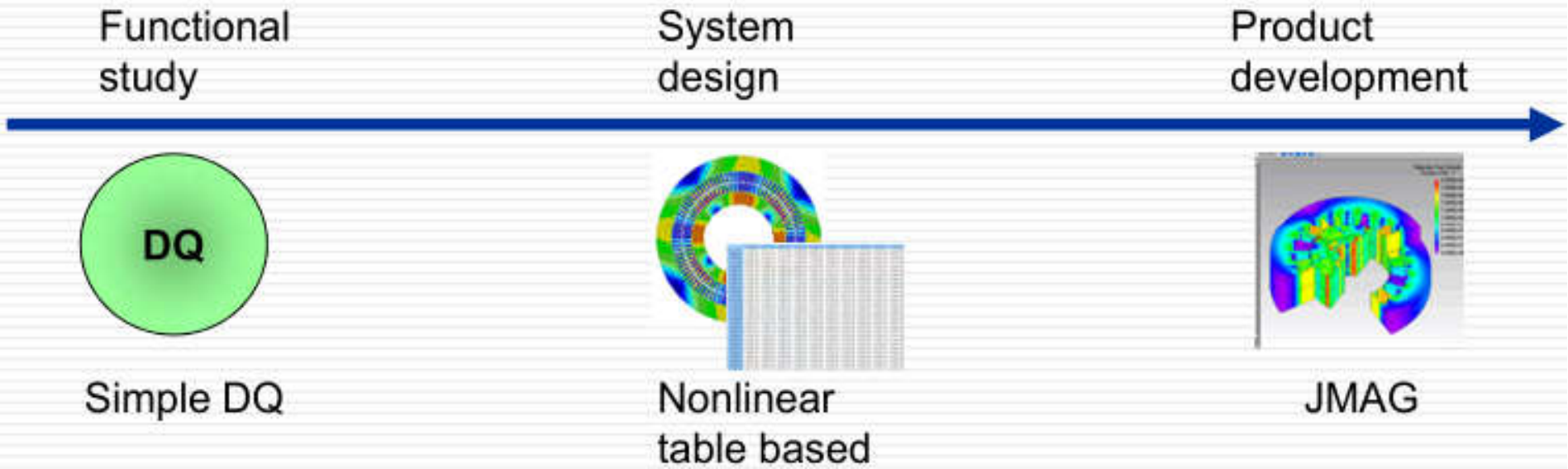
Rapid Control Prototyping



Hardware-in-the-Loop

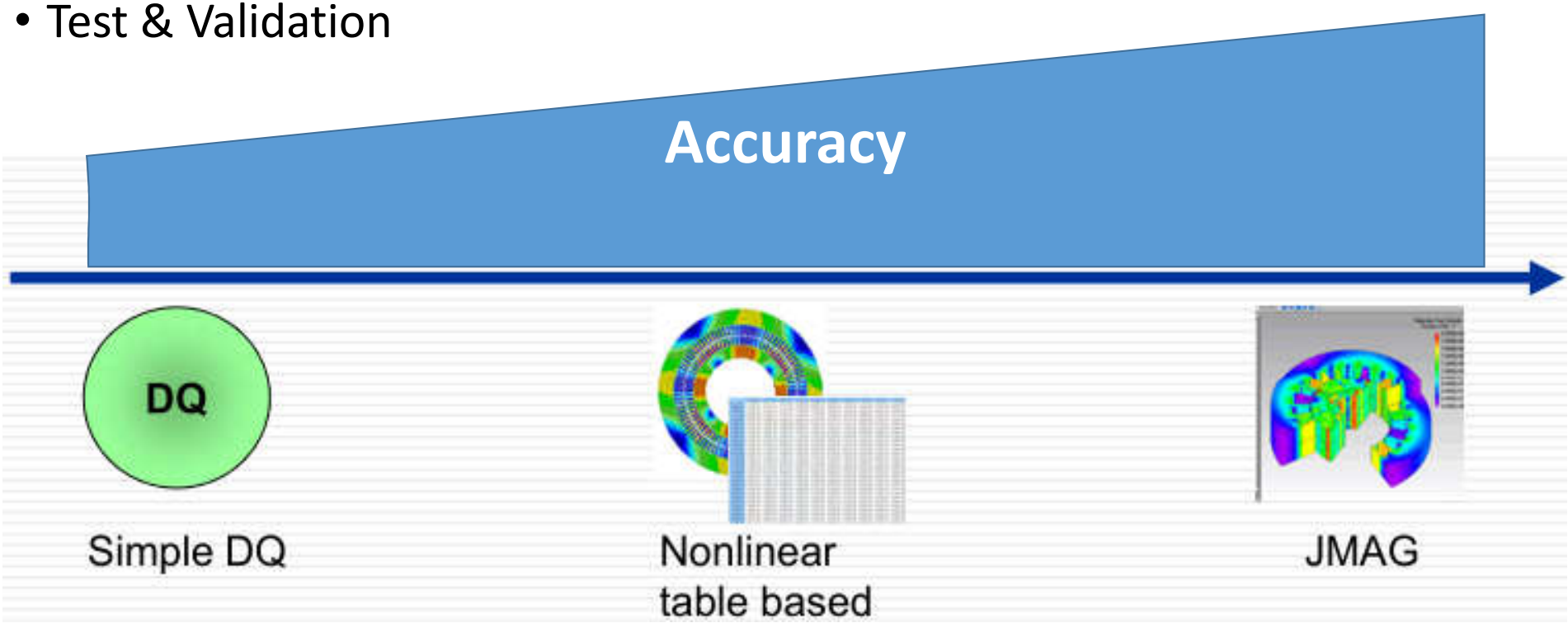


Hybrid Vechicle Development

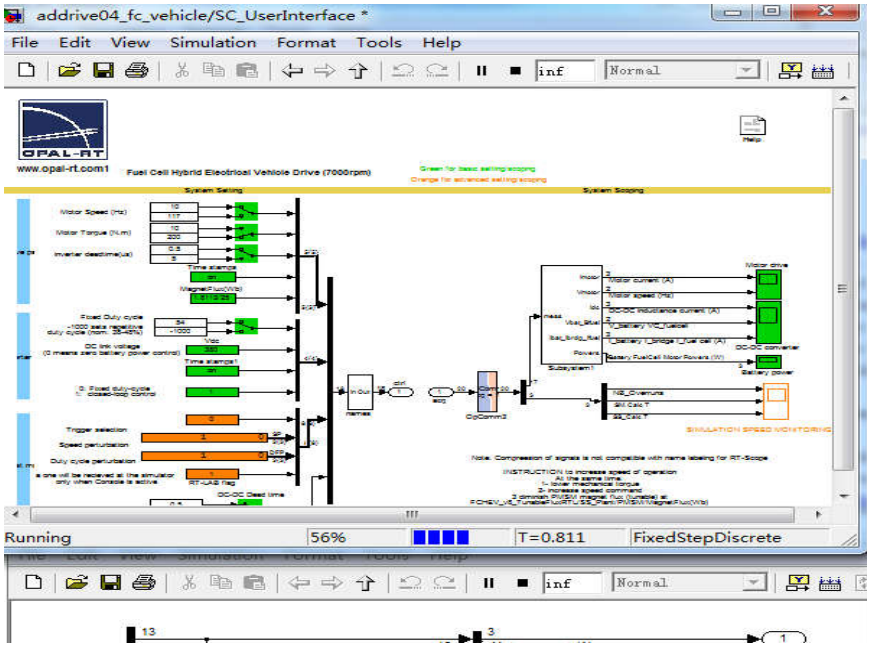


Hybrid Vechicle Development

- Test & Validation

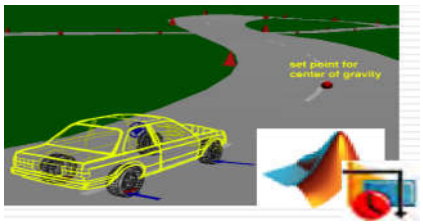


Simulation



Motivation to develop HIL

Simulation



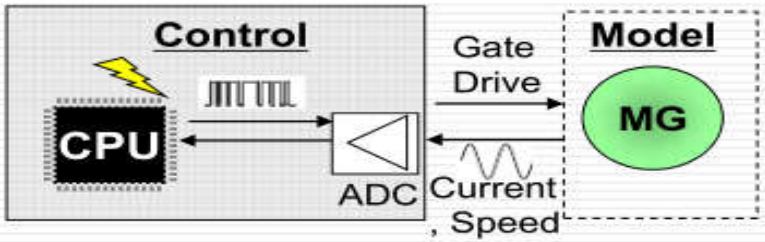
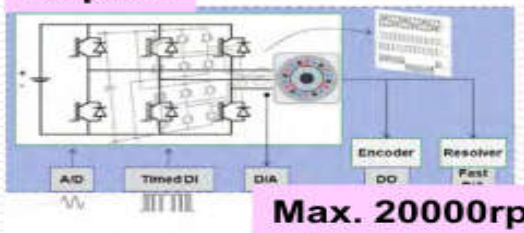
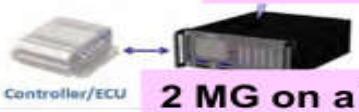
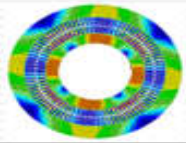
A large amount of automatic test
Easy to configure vehicle variation
Not the same result of the real vehicle

Vehicle

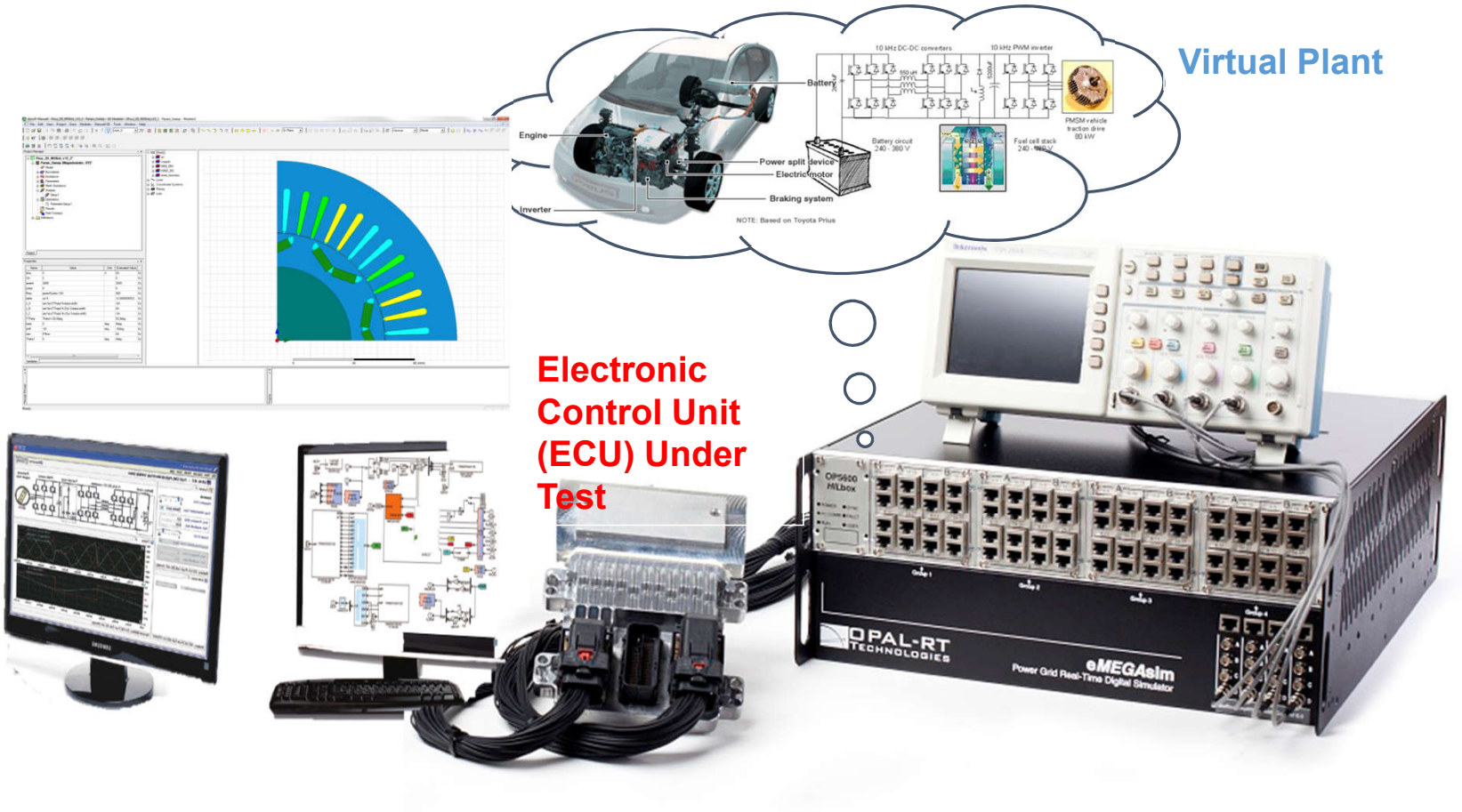
Need much human resources
Difficult to change configurations
Can get “Real” performance

- A large amount of automatic test
- Easy to configure vehicle variation
- Use real ECU to improve accuracy of Simulation

Hybrid Vehicle HIL

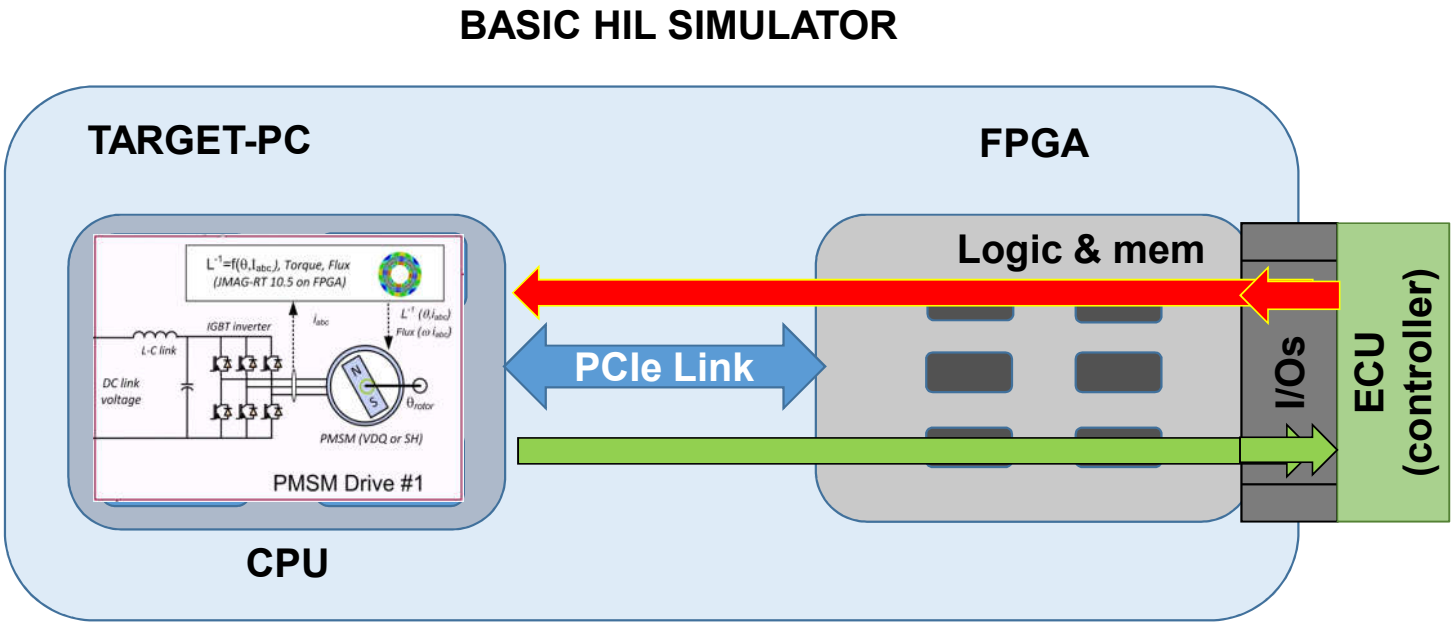
Requirement		Solution
Quick F/B response 	Less than 2μsec From input To output	  1.5μsec  Max. 20000rpm  2 MG on a Virtex 6
Max MG Speed	16000rpm	
Num of MG model	2 MG on 1 FPGA	
Torque vibration	Torque ripple , cogging	JMAG-RT 
Configurable vehicle	Easy to change configuration	FPGA (MG ,Inverter) + CPU (vehicle)

HIL for ECU Testing and Validation

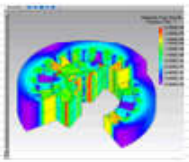


HIL Updating

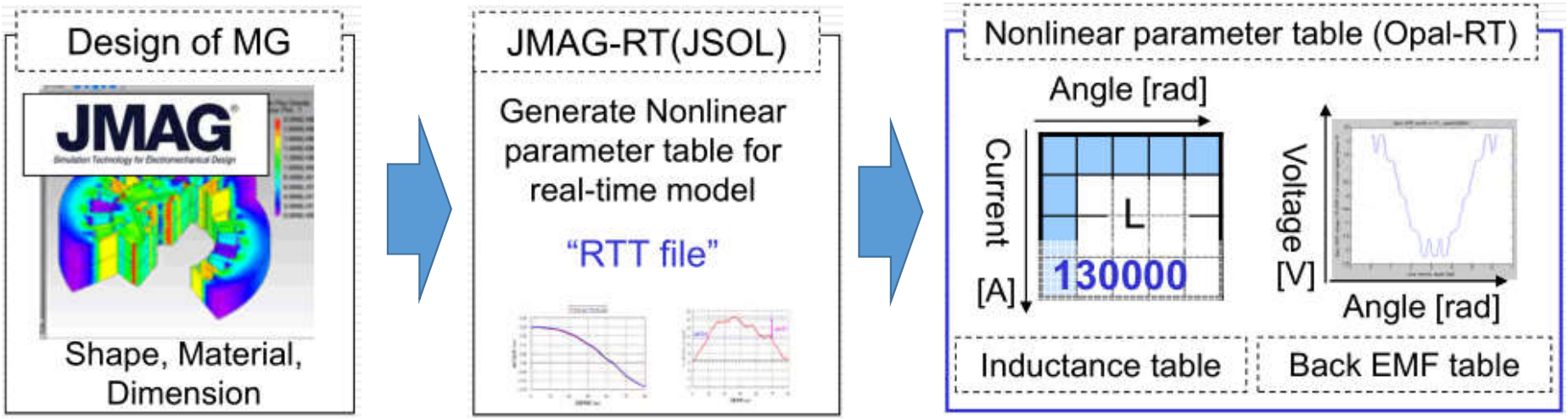
Role of FPGA in RT-LAB HIL



Problem of Model Development

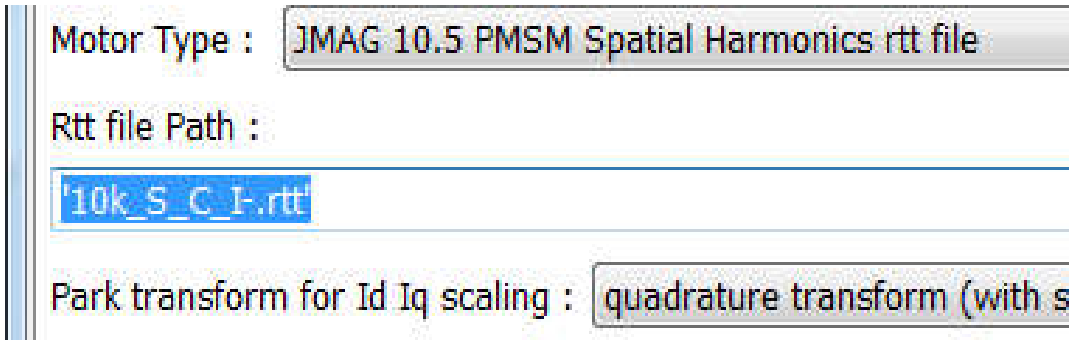
		DQ : (FPGA)	JMAG-RT : (FPGA)
Accuracy	Magnetic saturation	Not considered	Available
	Back EMF	Sinusoidal	Nonlinear
	Torque ripple	Not considered	Available
Time step		50nsec	25μsec → 50nsec
Parameter		**Easy to handle** Ld, Lq, R, lambda, …	**Difficult to obtain**  Hardware design parameter Shape, Material, Dimension, …

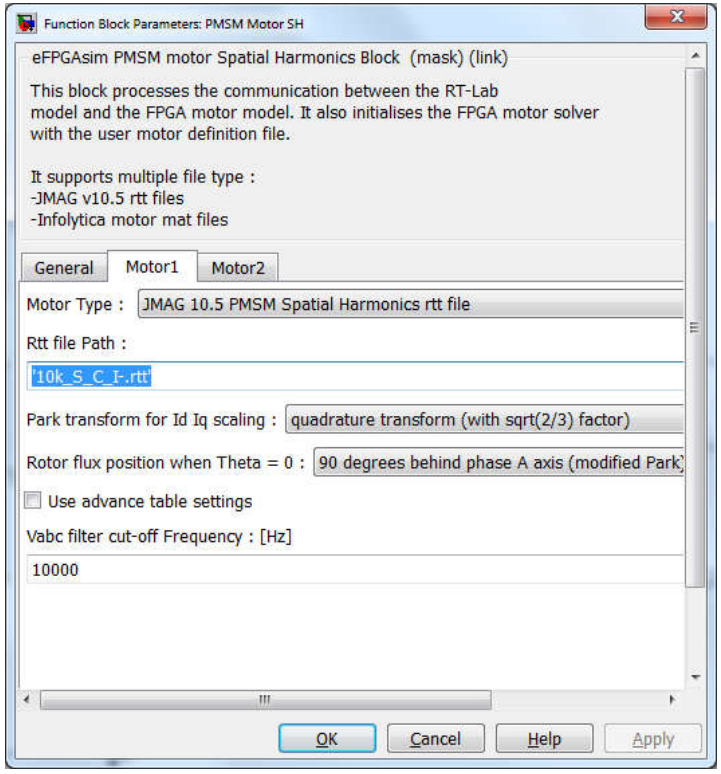
Process of JMAG-RT model parameterization



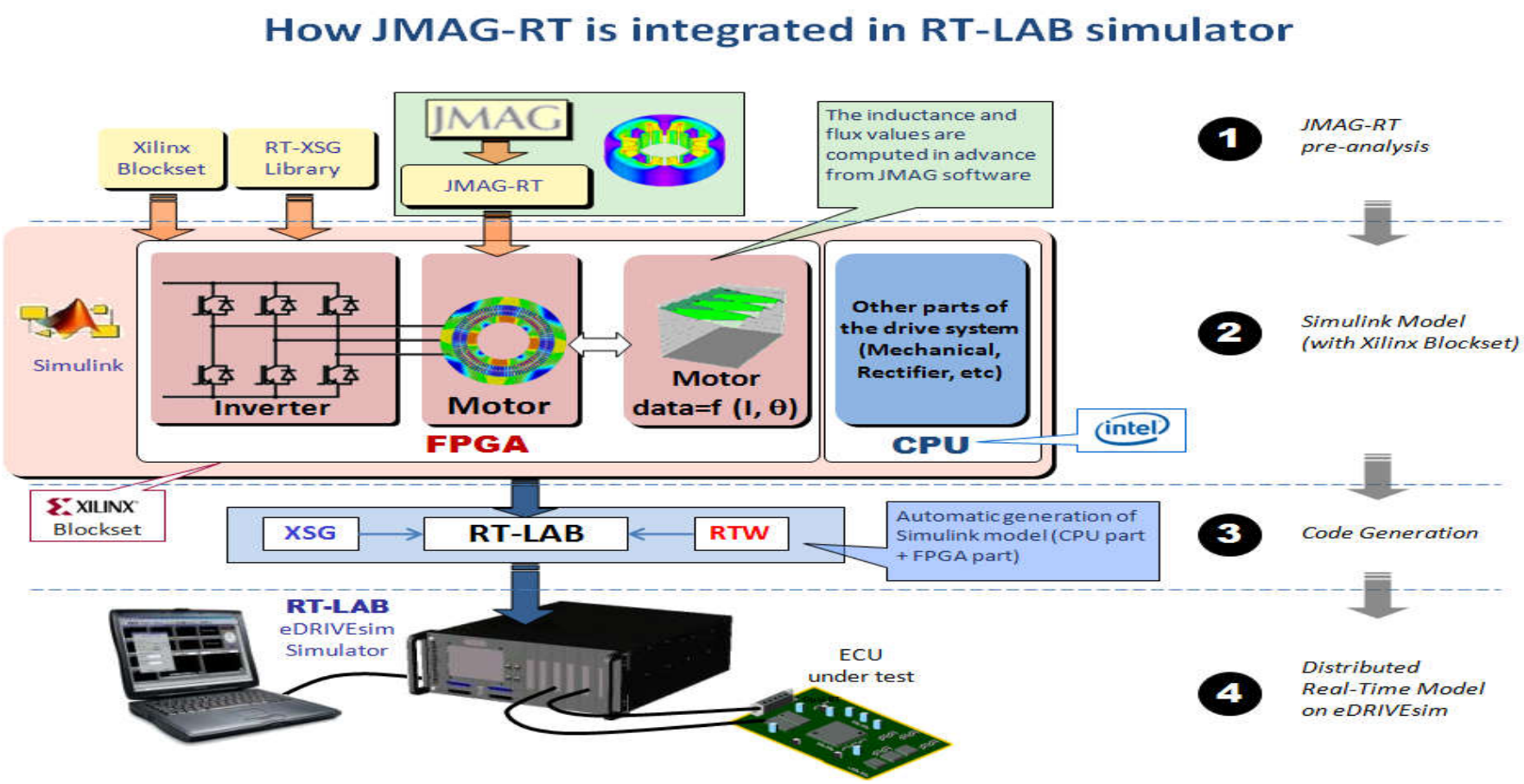
HIL System Flexibility: Non-Flashing technology

"Don't waste time re-generating a bitstream"

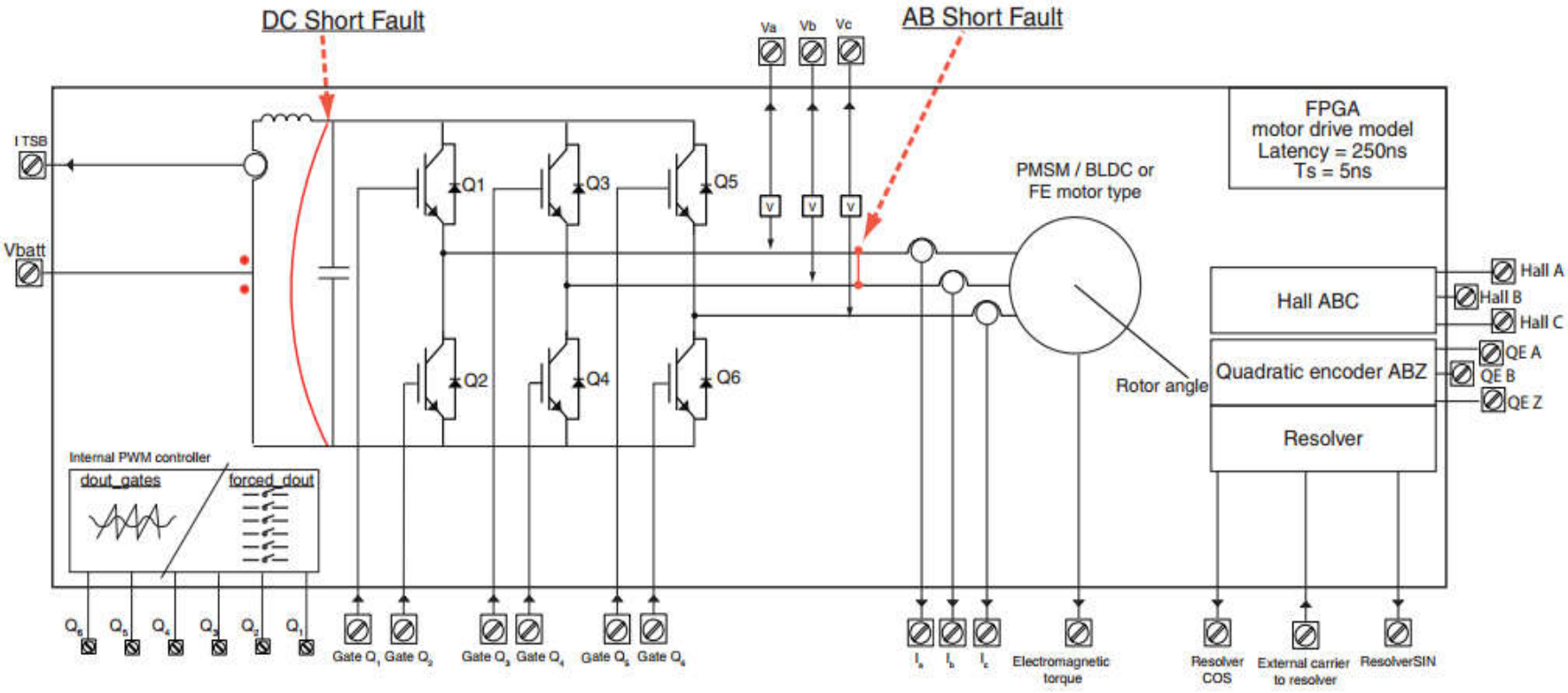




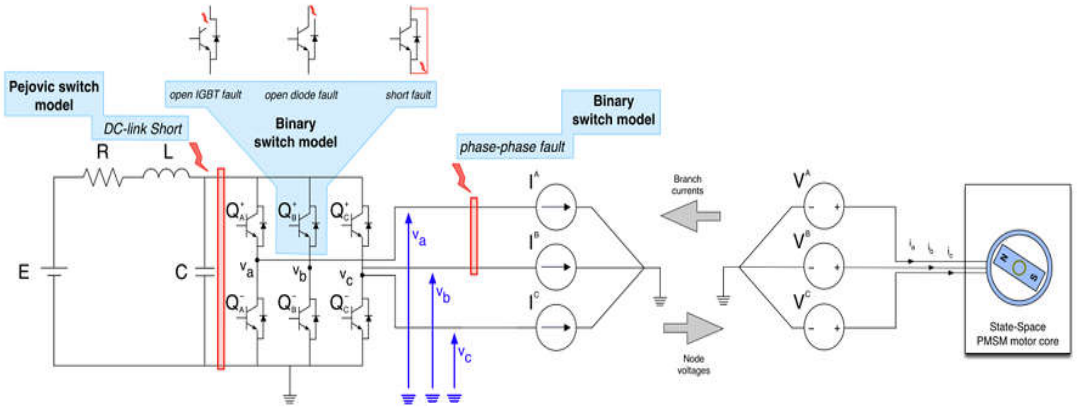
JMAG-RT in RT-LAB simulator



RT-LAB eFPGAsim



eFPGAsim FIU



Inverter faults	Motor and DC-link faults
Inverter IGBT open fault (any)	DC-link short-circuit
Inverter Diode open fault (any)	Motor phase-phase fault
Inverter IGBT & Diode open fault (any)	Motor open-phase fault
Inverter IGBT/Diode short circuit (any)	
No-gate signals at IGBT, with or without natural rectification	

Table 3: List of supported faults for the FPGA motor drive

Outline

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Successful stories

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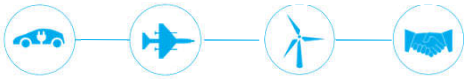
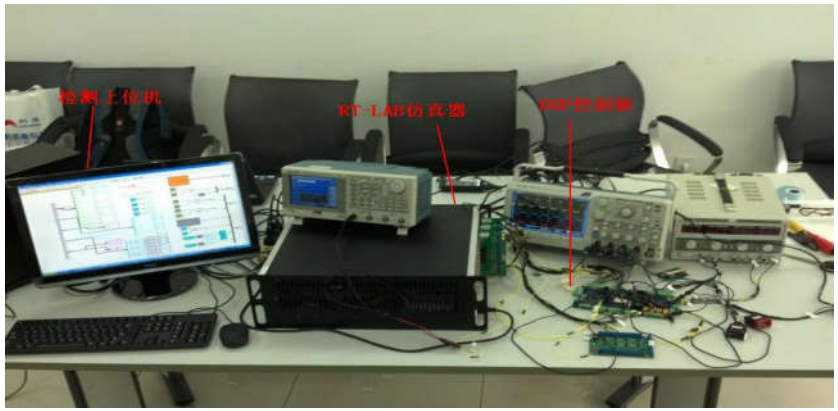
Products and service

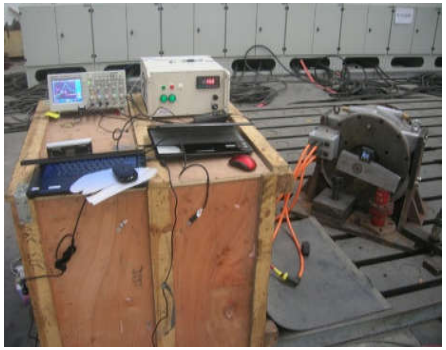


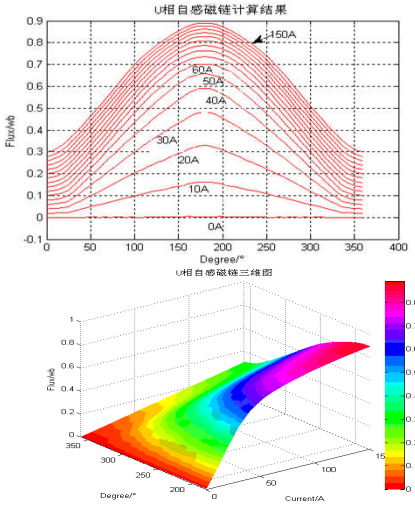
Ford

- Challenging requirements for PMSM electric-drive simulation with IGBT inverters
  - PWM signals in the 2-20 KHz range
  - 2-20 µs dead-time
  - Typical real-time simulation sample times cannot capture switching events and provide accurate transient simulation
  - Opal-RT eDRIVEsim solution with fast I/O using FPGAs (10 ns resolution for digital I/O and 1 µs conversion time for analog signals)
  - Opal-RT's real-time inverter and PMSM models using the time-stamped averaging method (TSAM) used for accurate simulations

RM HIL





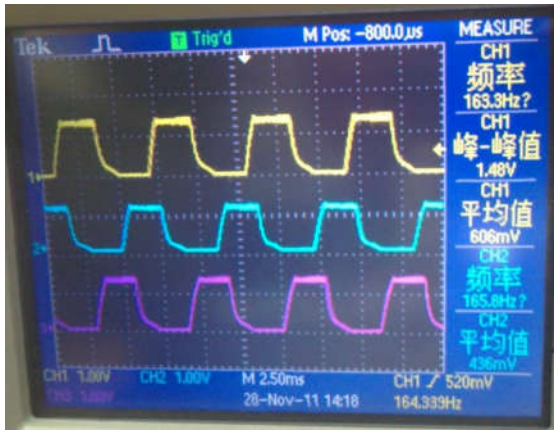


硬件在环-有限元电机模型实现

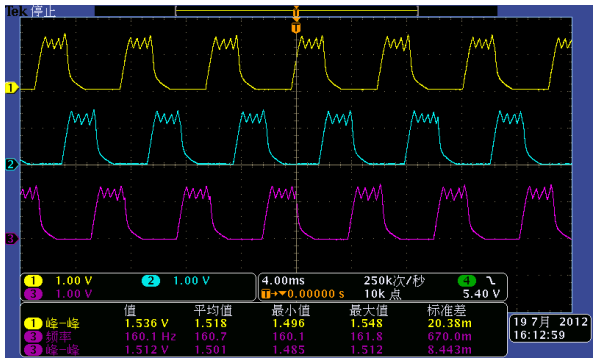
- 实验结果对比
  - 电流波形对比：
  - 指标：额定工况下相电流波形对比误差<8%。
  - 对比结果：误差为3.55%，满足要求。

	台架测试	硬件在环测试
相电流波形峰-峰值	1.48V	1.53V
电流值	197.3A	204A
转速	800rad	800rad
功率	40KW	40KW
对比误差		3.55%

实测电机波形

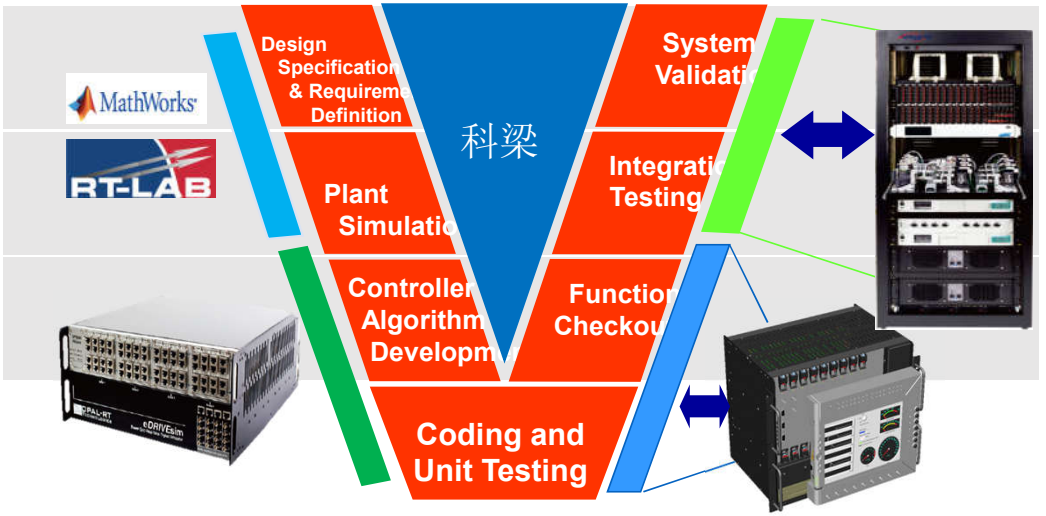


硬件在环测试波形



Summary

- 实现快速原型开发和硬件在环测试统一的工具链
- 软件RT-LAB
  - 规范易用的模型分核分布计算，内部节点通信和信号IO模块
  - “Six Clicks to Real-Time”用户界面
- 高速硬件资源
  - 10ns的IO
  - FPGA高速运算技术
- 高精度的电机&
- 电子元器件库
  - DQ，VDQ， JMAG-RT
  - IGBT（FI)



Thank You!