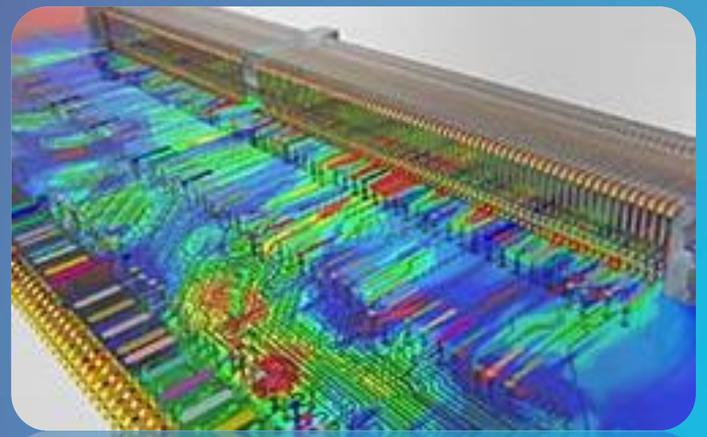

ANSYS SIwave信号完整性仿真基础及新功能介绍

艾迪捷信息科技（上海）有限公司
IDAJ-CHINA
高频电磁场技术经理 资深高频技术工程师 刘捷

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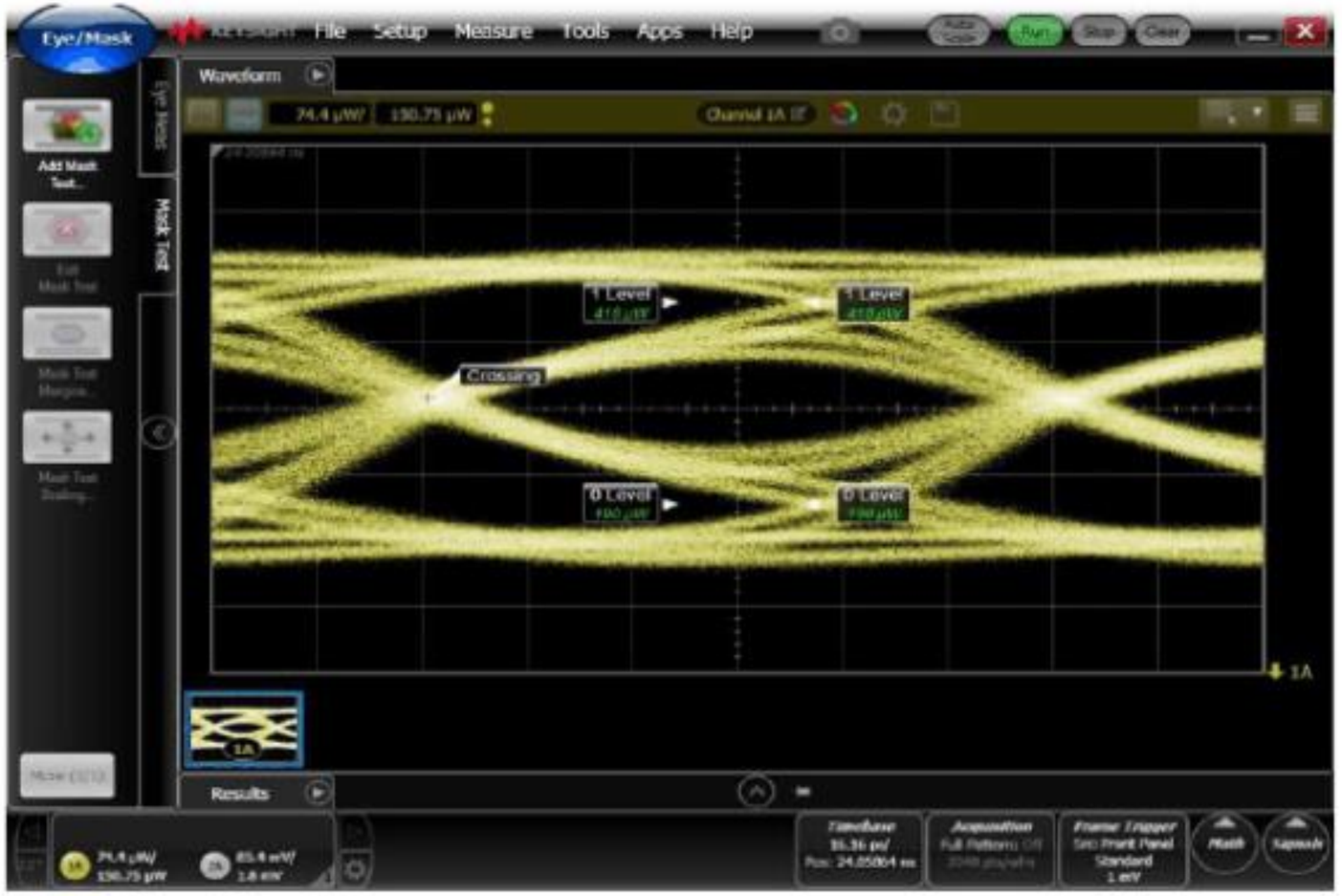
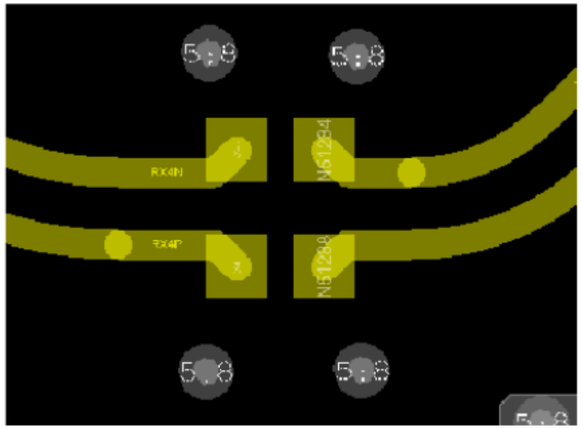
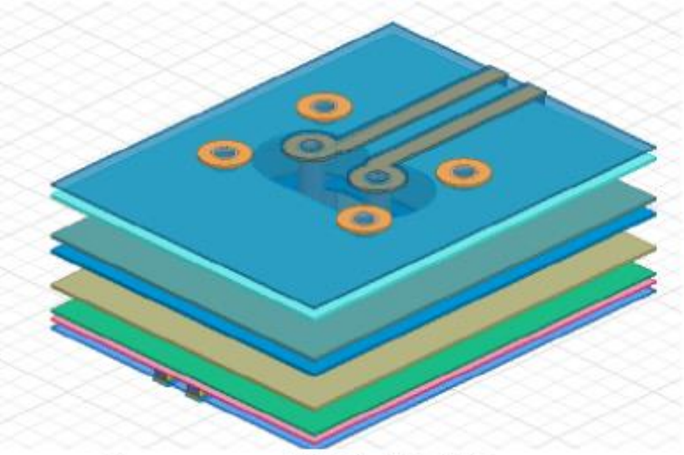
信号完整性设计案例



信号完整性设计案例



器件焊盘走线阻抗不连续



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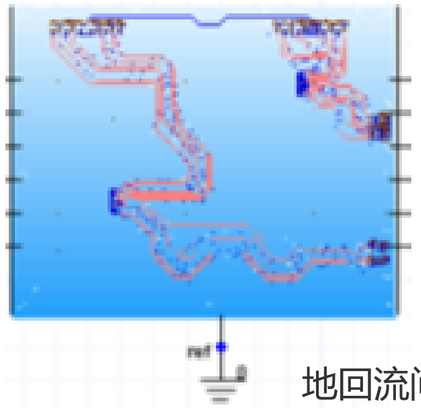
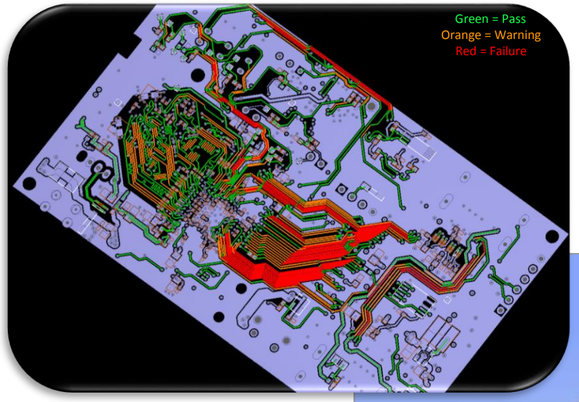
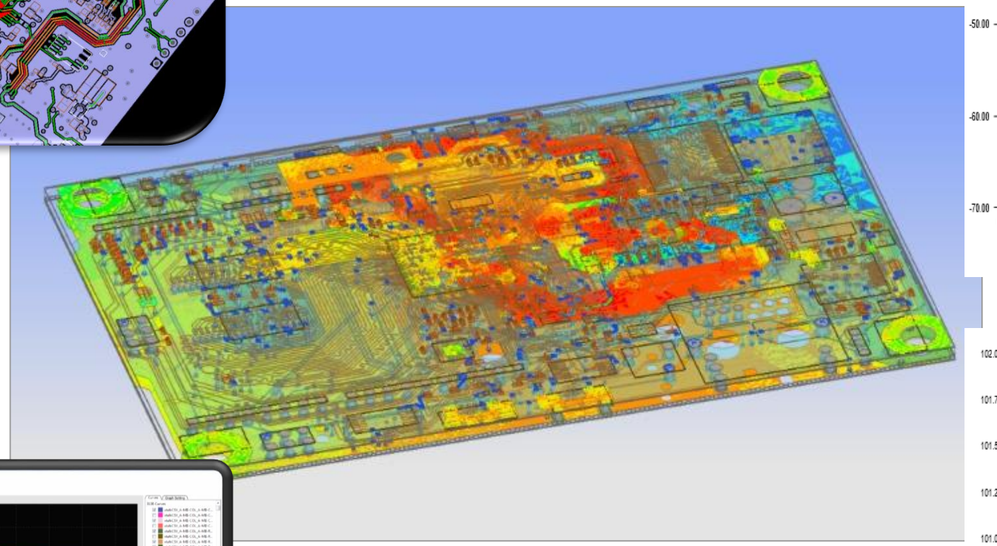
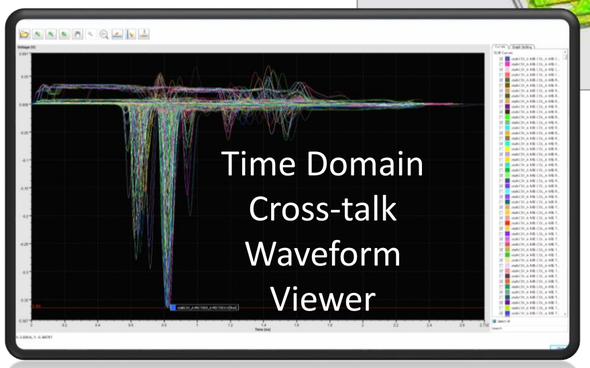


地回流问题

信号完整性设计案例







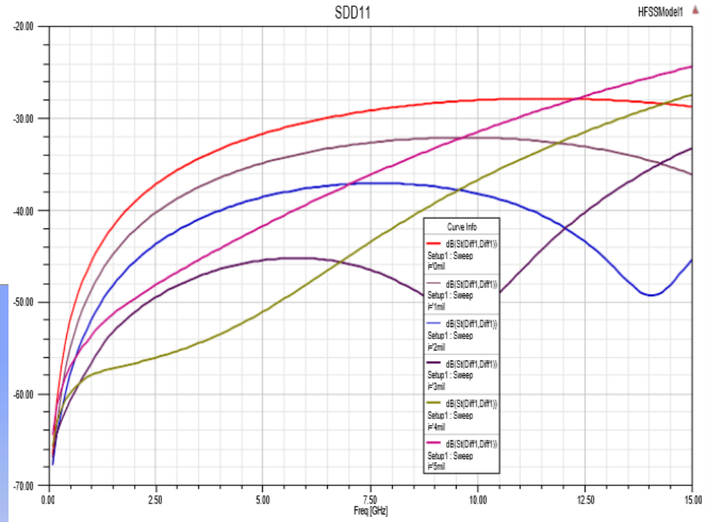


图 6（回波损耗）

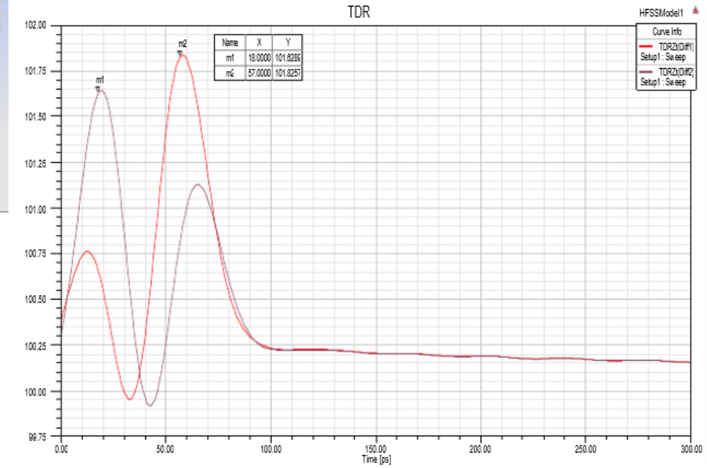
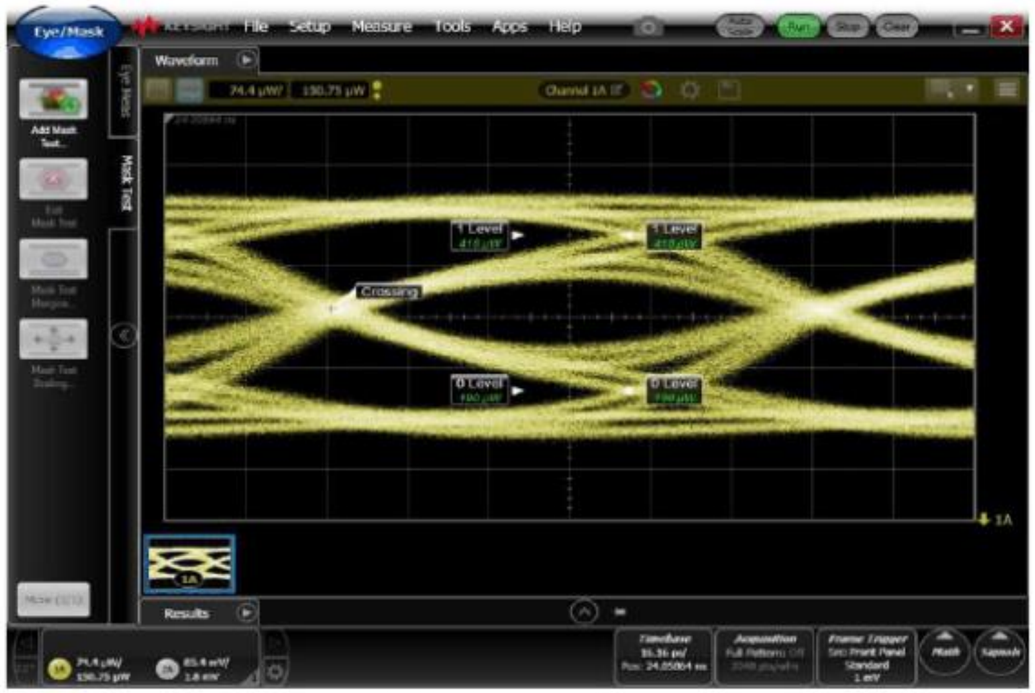
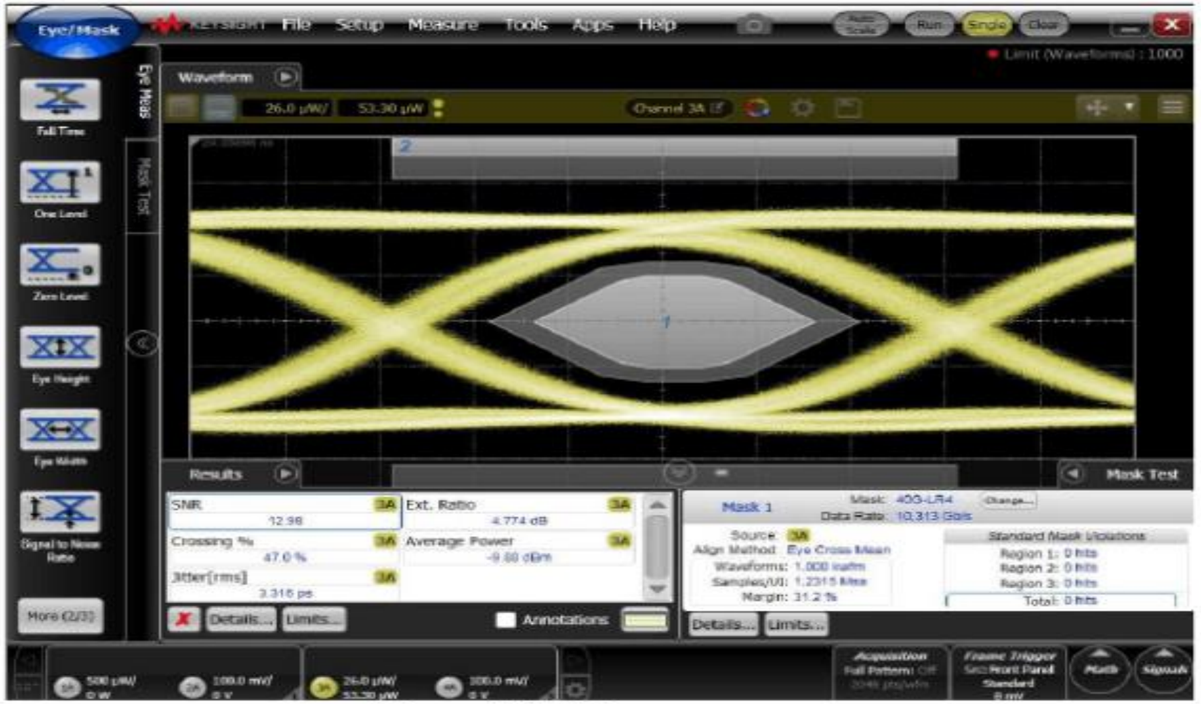


图 10（TDR，99-102Ω之间）

信号完整性设计案例

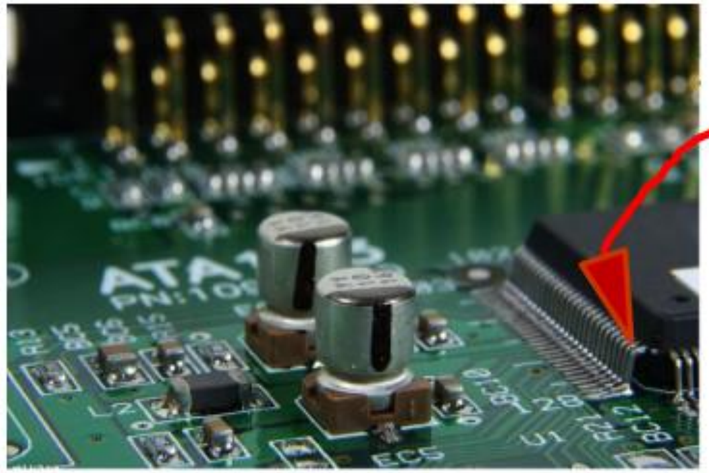


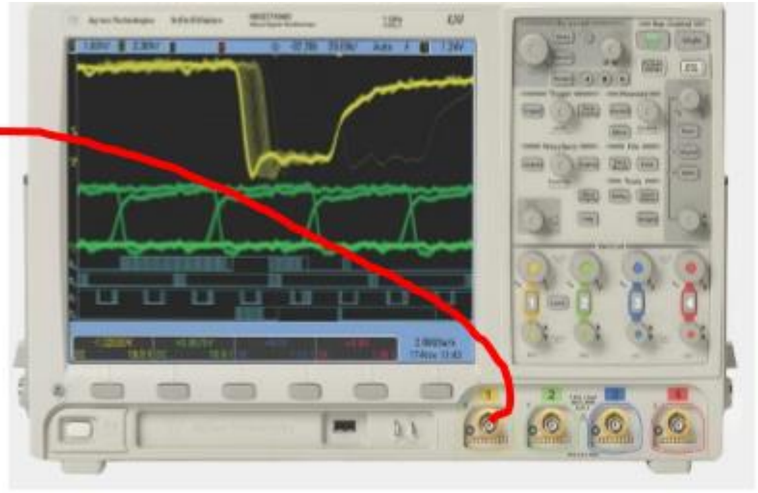
优化前眼图

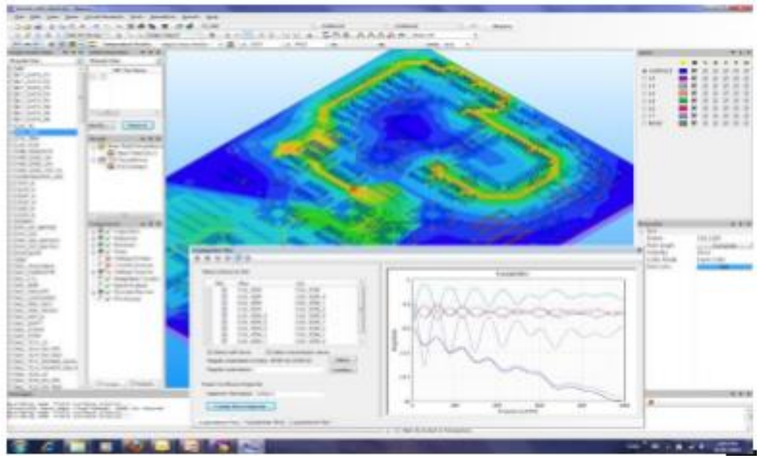


优化后眼图

PCB电源噪声干扰案例



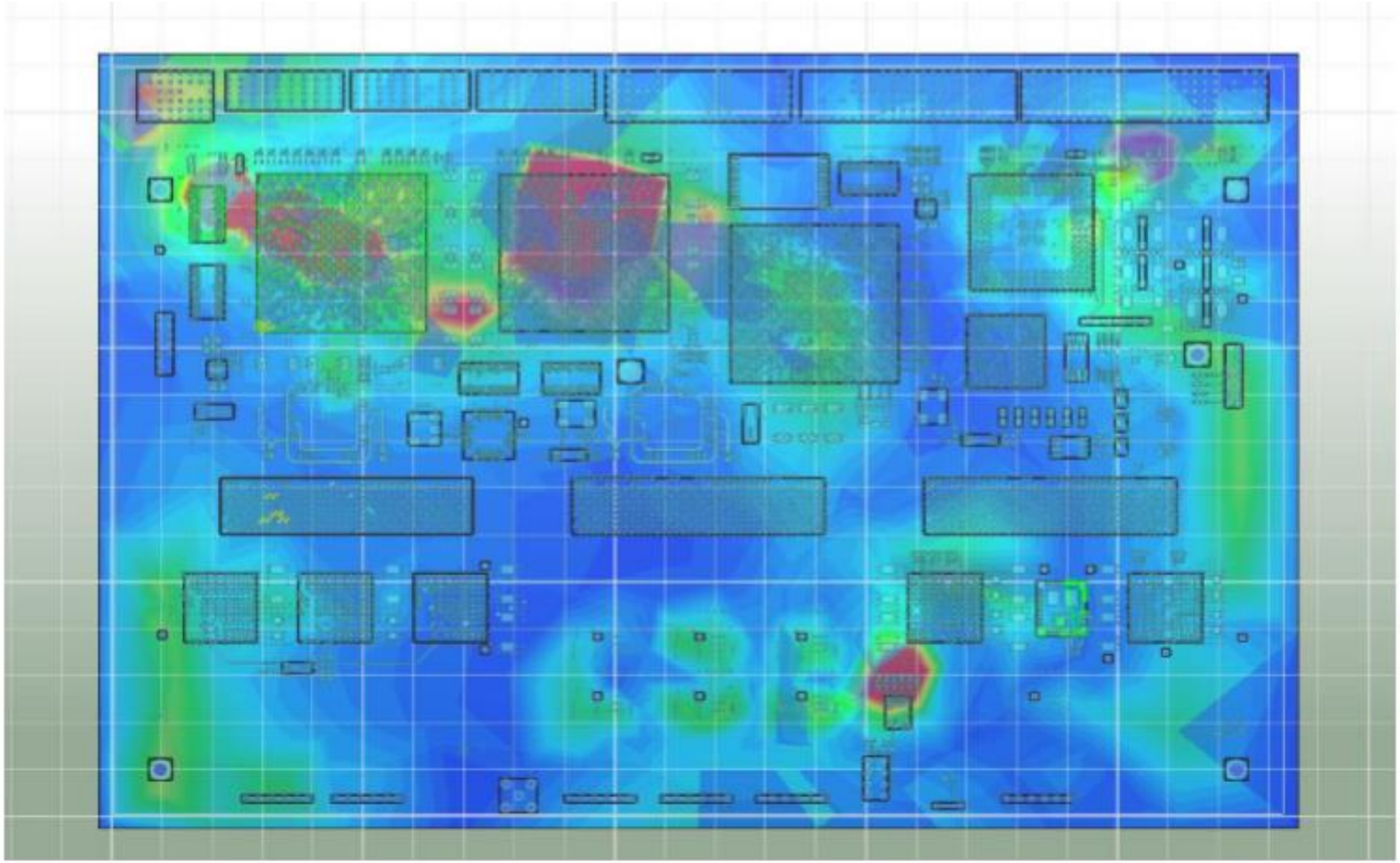




测试发现芯片电源电路附近存在较大噪声

原始PCB布线导入SIwave

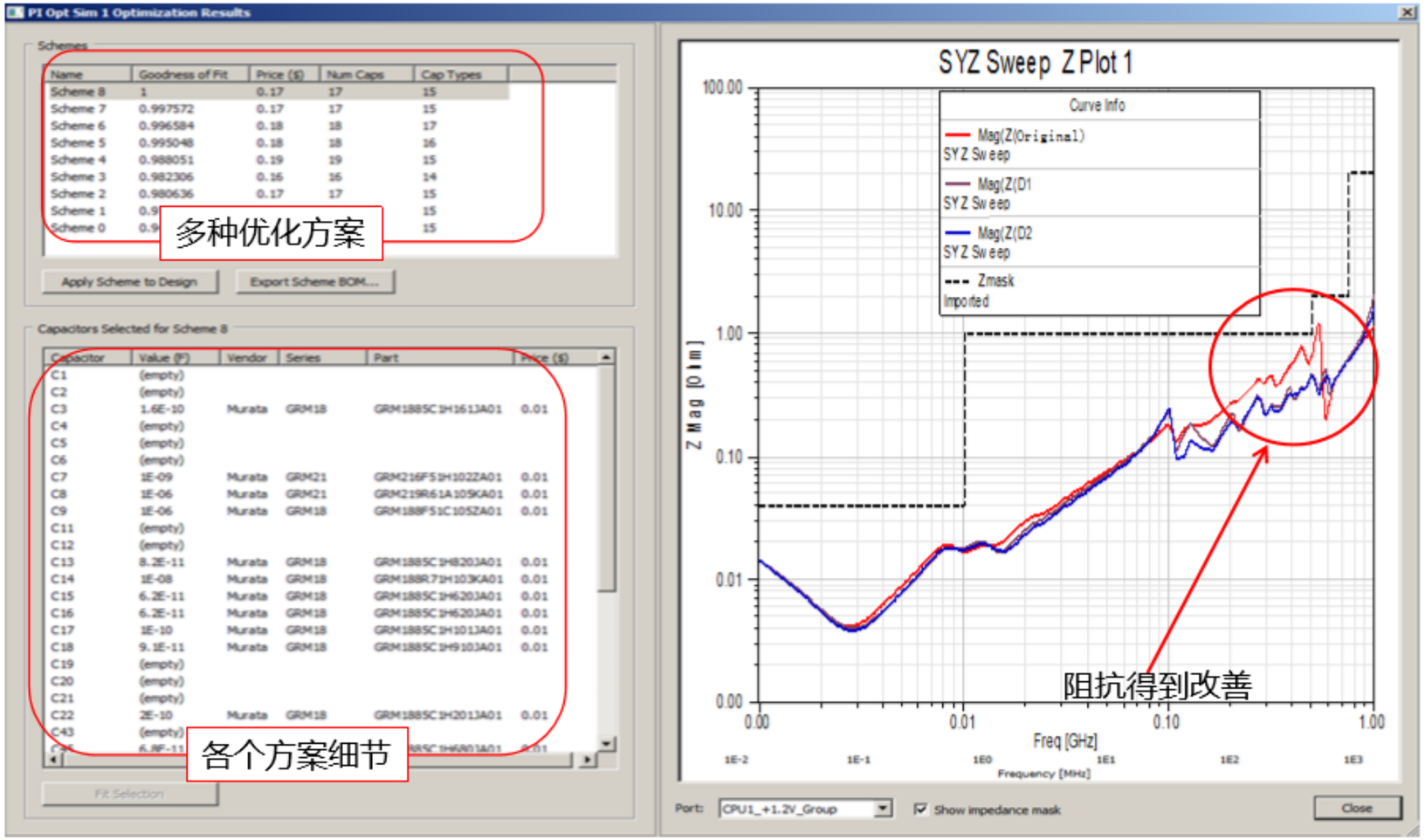
PCB电源噪声干扰案例



近场辐射分布

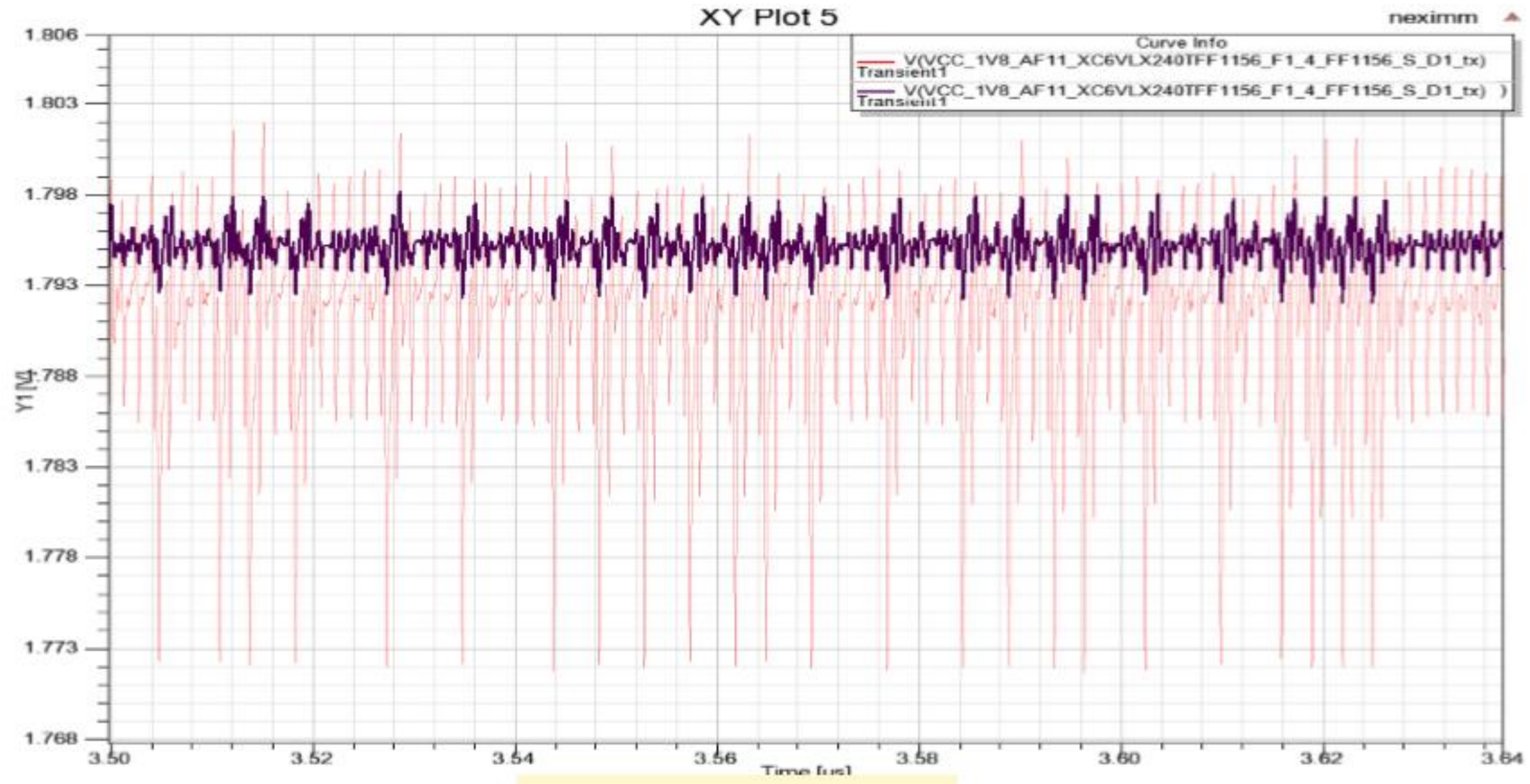
PCB电源噪声干扰案例

电源平面目标阻抗优化结果



PCB电源噪声干扰案例

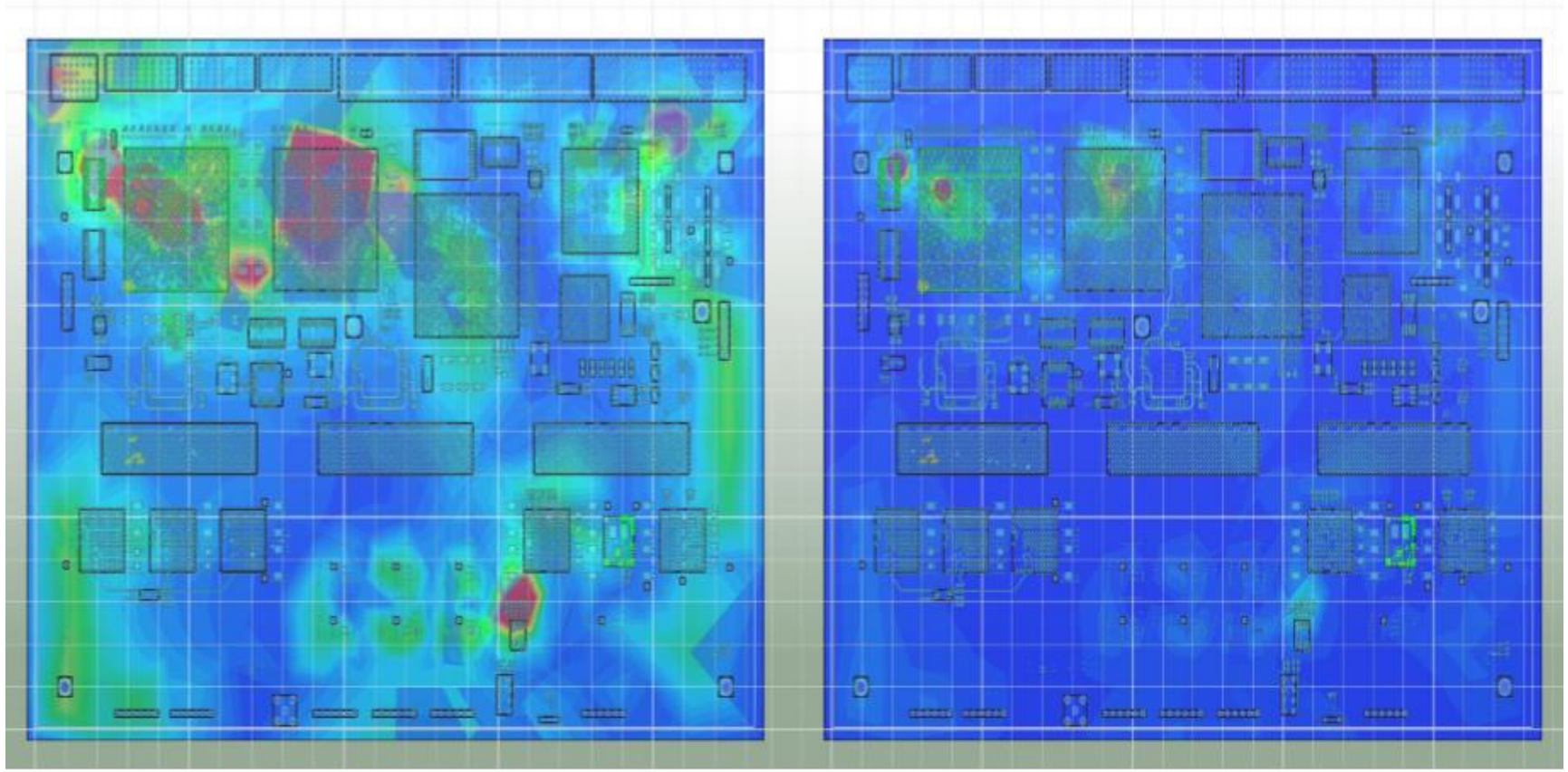
电源时域抖动改善



电源波动-优化前后对比

PCB电源噪声干扰案例

PCB近场优化对比



PCB电源优化前　　PCB电源优化后

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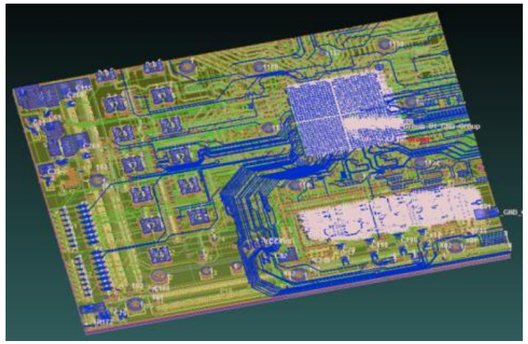
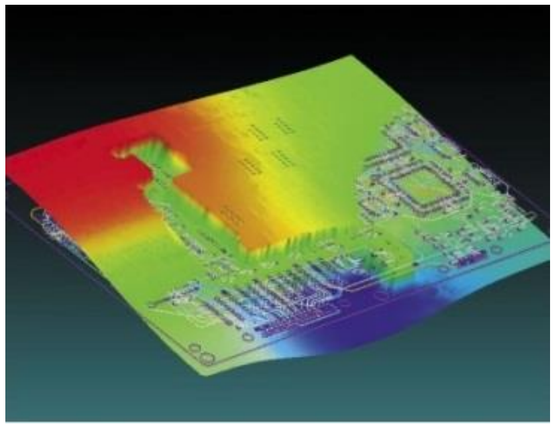
ANSYS SIwave

SIwave是特别针对**PCB、芯片封装的SI/PI/EMC仿真**工具，采用定制化的电磁场算法, 能够高效准确地求解几十层的PCB和上千管脚的封装结构。

功能特点

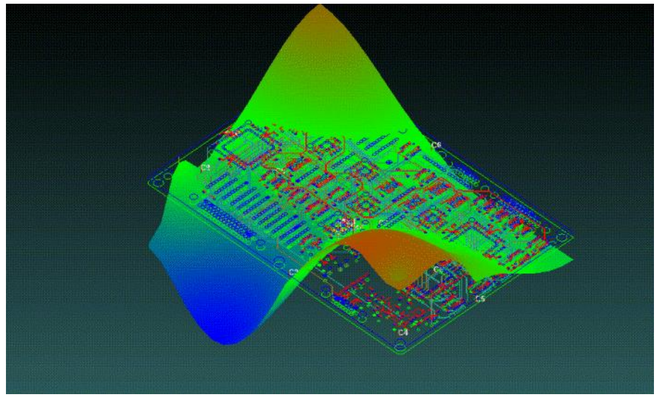
- 与EDA设计工具无缝集成
- 涵盖PCB从直流设计到去耦电容设计，从高速设计到EMC设计所有方面
- 帮助工程师深刻洞察电路器件与电磁场器件的相互作用
- 自动考虑PCB板上所有互连结构，如走线、过孔和焊盘等



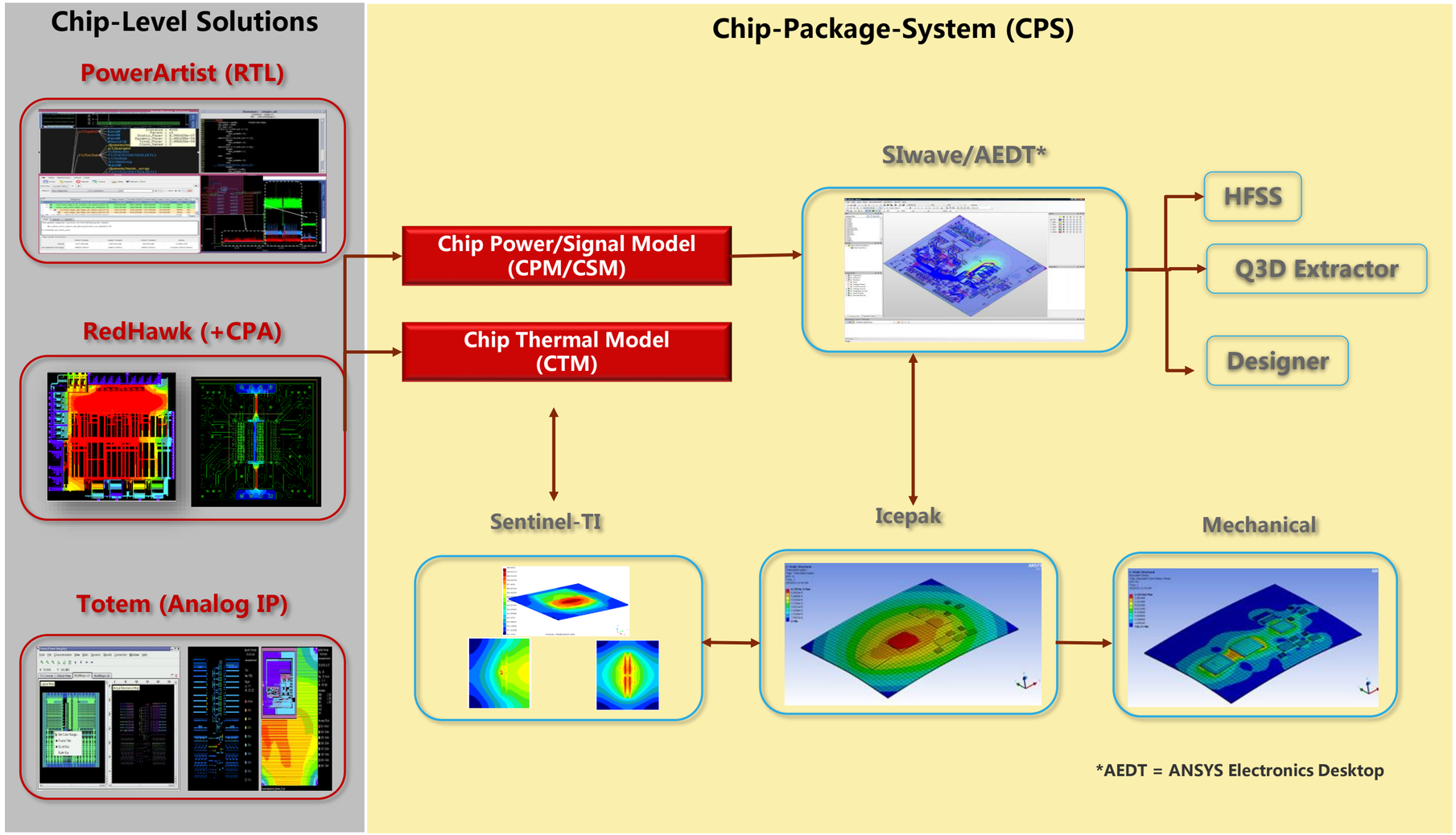


应用领域

- 集成电路 (IC) 封装
- PCB 直流分布、SI、PI
- 去耦电容自动优化
- 高速通道设计
- 近远场辐射、EMI/EMC



ANSYS Chip-Package-System Solutions



ANSYS SIwave

- *Cadence*
- *Mentor Graphics*
- *Altium*
- *Zuken*

Layout Generated in ECAD System

Drawing Editor

Analyzer [Hybrid 2.5D full wave EM field solver]

DC Analysis

- *I²R Drop*
- *Current Distribution*
- *Signal Flow Graph*
- *Thermal Coupling with IcePak*

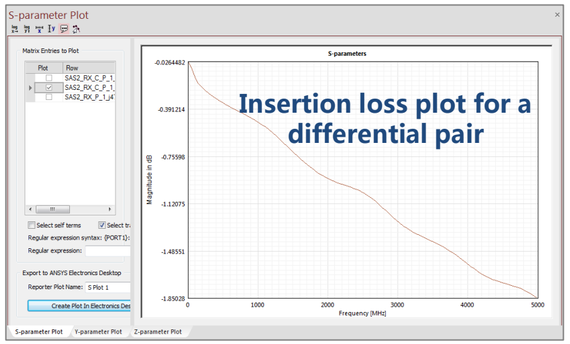
AC Analysis

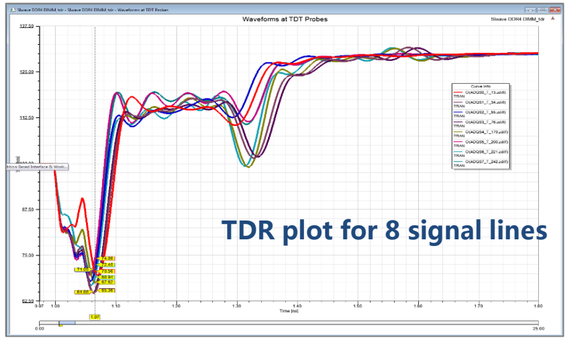
- *AC Impedance analysis*
- *S-Parameter extraction*
- *Near and Far Field Extraction*
- *Crosstalk analysis*
- *Capacitor Optimization*

Resonant Modes

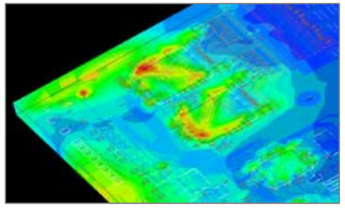
SPICE Models

- *Nexxim*
- *HSPICE*
- *Cadence Spectre*
- *PSPICE*
- *Maxwell Spice*



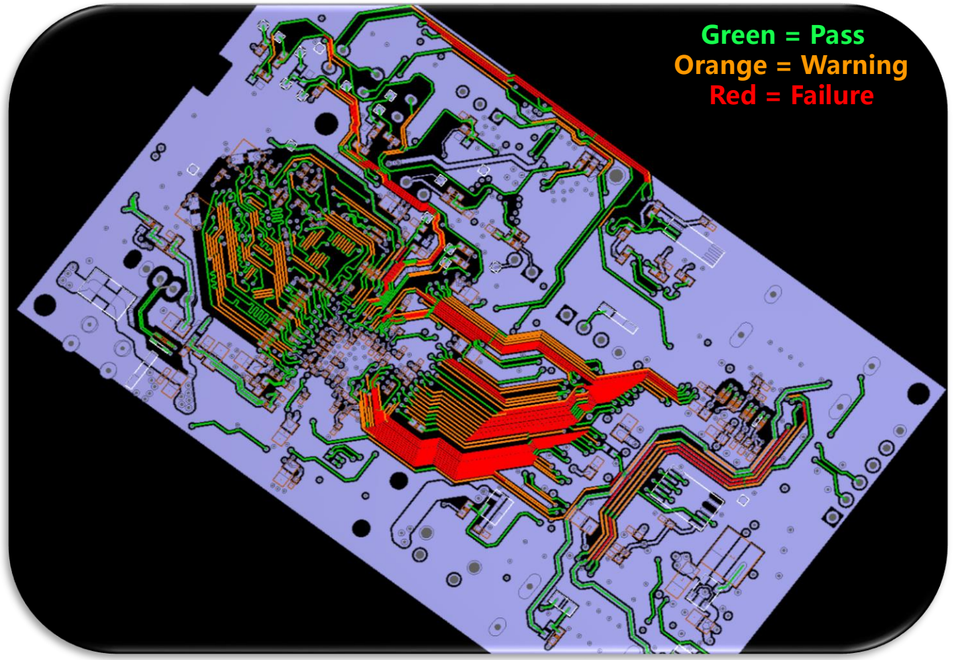


Prediction of EMI on a dual-processor quad-core PCB. Plot depicts near-field magnetic field at 778 MHz



Hybrid solver technology enables simulation of entire system (PCB and Package)

ANSYS SIwave——Layout Scanning



NEXT coefficient

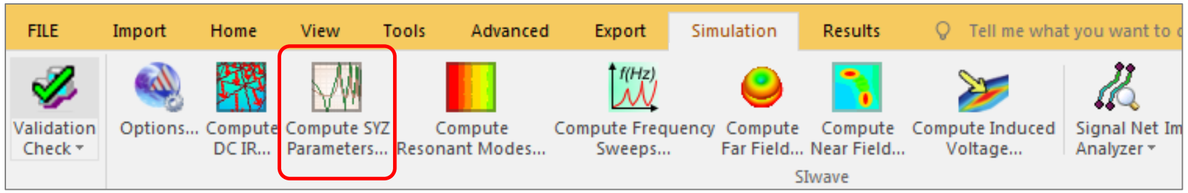
Net Name	NEXT Warning Tolerance	NEXT Violation Tolerance	SE or Diff	Cross Section Type	Violation	Layer of Violation	Max NEXT	Length of Max NEXT (mm)	NEXT of Longest Line Section	Length of Longest Line Section (mm)
VSYNC_STB	0.1	0.2	SE	MSL; STL	No		0.06	2.071	0.024	8.644
V_HDMI_5V	0.1	0.2	SE	MSL; STL	No		0.044	2.52	0	11.009
XMMCCLK0	0.1	0.2	SE	MSL; STL	No		0.1	1.295	0.031	14.542
XMMCCMD0	0.1	0.2	SE	MSL; STL	No		0.1	1.854	0.066	9.626
XMMCDATA0_0	0.1	0.2	SE	MSL; STL	No		0.099	3.128	0.078	18
XMMCDATA0_1	0.1	0.2	SE	MSL; STL	No		0.098	3.033	0.035	14.573
XMMCDATA0_2	0.1	0.2	SE	MSL; STL	No		0.1	1.295	0.031	14.542
XMMCDATA0_3	0.1	0.2	SE	MSL; STL	No		0.097	8.941	0.031	14.549
XNRESET	0.1	0.2	SE	MSL; STL	No		0.099	5.984	0.016	23.085
XOTGD	0.1	0.2	Diff	MSL; STL	No		0.001	7.57	0	8.027
XOTGD_EMI	0.1	0.2	Diff	MSL; STL	No		0	1.85	0	1.85
XOTGID	0.1	0.2	SE	MSL; STL	No		0.011	1.278	0	9.888
XURXD_0	0.1	0.2	SE	MSL; STL	No		0.084	1.47	0	7.186
XUSBHD	0.1	0.2	Diff	MSL; STL	No		0	6.116	0	6.116
XUTXD_0	0.1	0.2	SE	MSL; STL	No		0.083	2.842	0	7.687
XVBUS	0.1	0.2	SE	MSL; STL	No		0	7.793	0	7.793

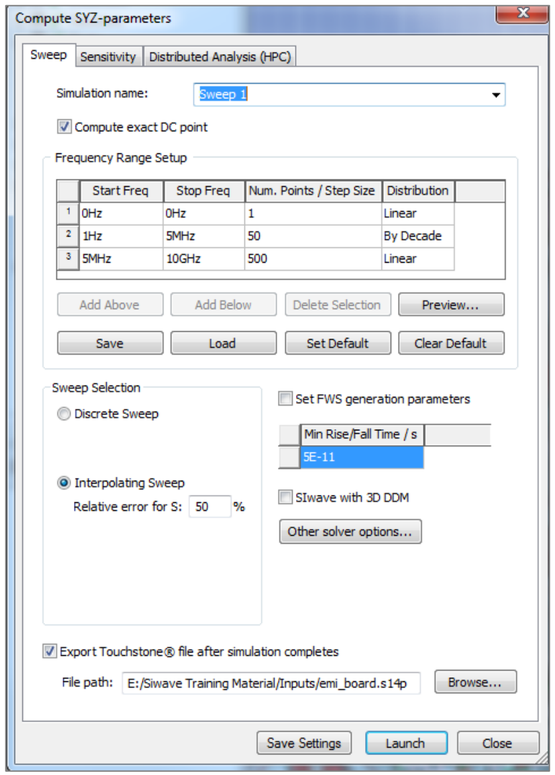
FEXT coefficient

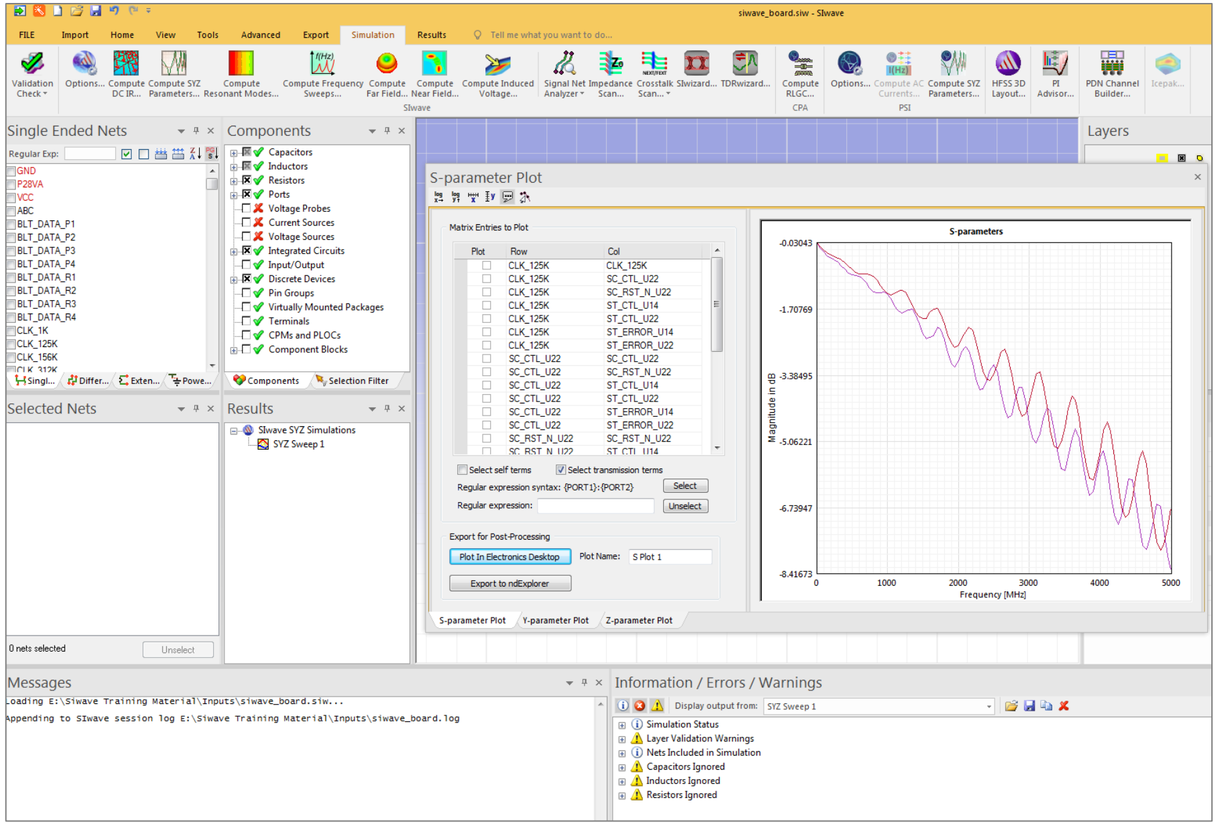
Net Name	FEXT Warning Tolerance (ns/m)	FEXT Violation Tolerance (ns/m)	SE or Diff	Cross Section Type	Violation	Layer of Violation	Max FEXT (ns/m)	Length of Max FEXT (mm)	FEXT of Longest Line Section (ns/m)	Length of Longest Line Section (mm)
						"top"	0.227	6.43	0.227	6.43
AP_TCK	0.1	0.2	SE	MSL; STL	Yes	"bottom"	0.205	3.268	0.205	3.268
AP_TDI	0.1	0.2	SE	MSL; STL	Yes	"bottom"	0.214	7.902	0.214	7.902
AP_TDO	0.1	0.2	SE	MSL; STL	Yes	"bottom"	0.219	4.037	0.204	8.152
						"top"	0.209	12.456	0.209	12.456
AP_TMS	0.1	0.2	SE	MSL; STL	Yes	"bottom"	0.205	1.425	0.205	1.425
AP_TRST	0.1	0.2	SE	MSL; STL	Yes	"bottom"	0.218	1.767	0.202	7.228
CEC	0.1	0.2	SE	MSL; STL	Yes	"bottom"	0.203	8.142	0.203	8.142

Full PCB Zo and NEXT/FEXT Scanning Capabilities

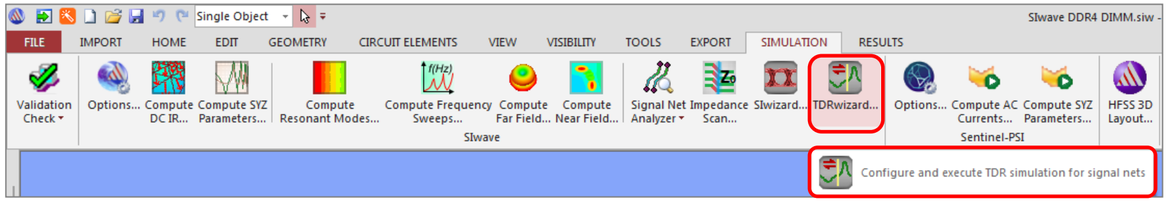
ANSYS SIwave——S parameter

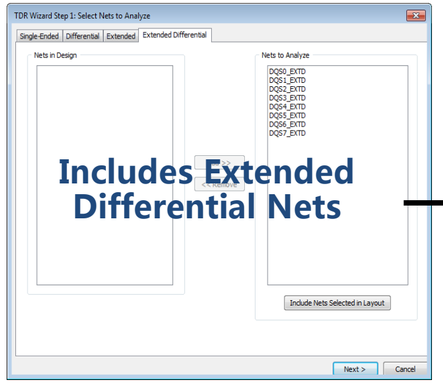


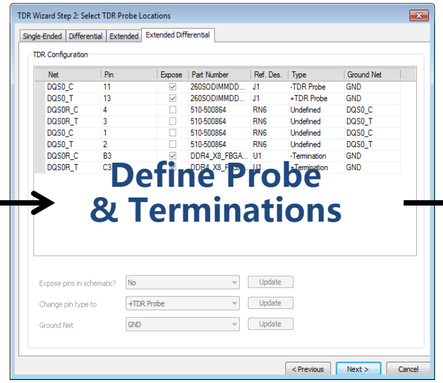


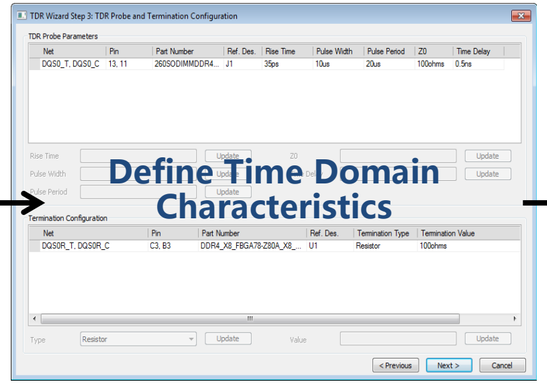


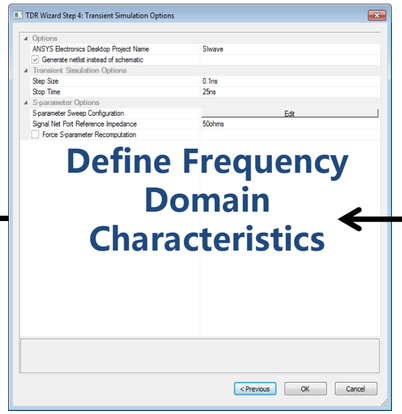
ANSYS SIwave——TDR

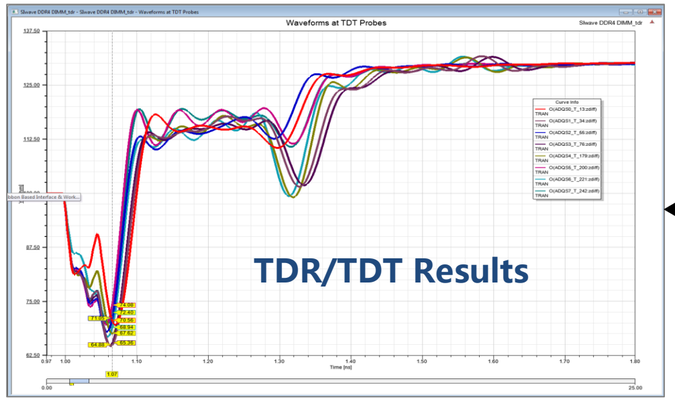












ANSYS SIwave——Time domain Simulation

Circuit Simulation using Nexxim

– Schematic entry GUI or Netlist entry (user choice)

Supports

– HSPICE netlists, Spectre netlists, and Spectre RF netlists

Simulation Engines

– Nexxim (SI focused analyses)

Linear network analysis (SYZ network analysis)

Causality checking and enforcement

Passivity checking and enforcement

TouchStone viewing and matrix reduction

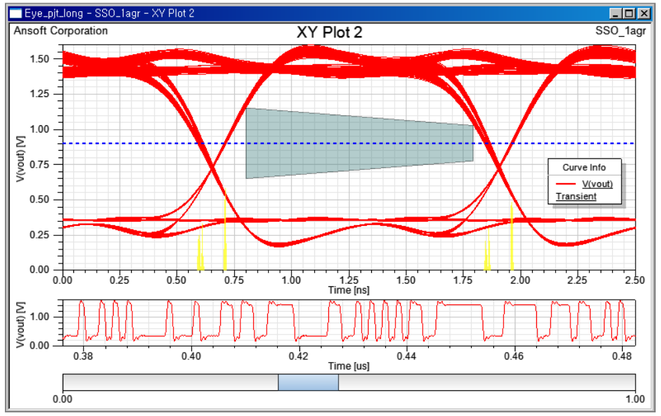
Traditional Transient

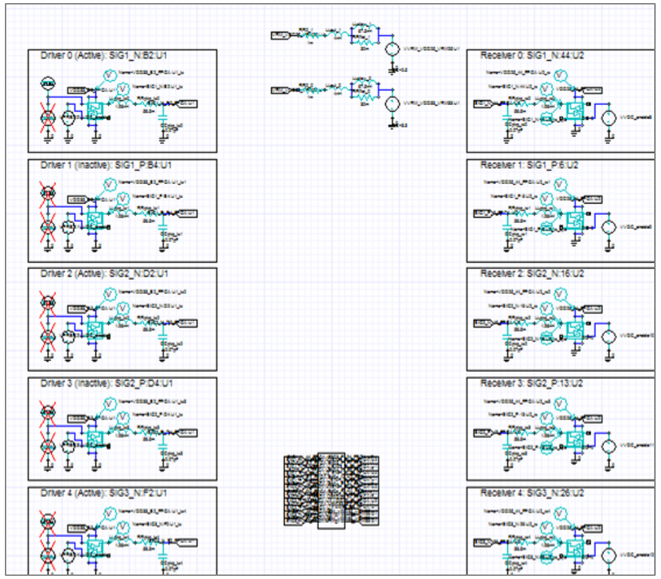
QuickEye (Convolution bit pattern based approach)

Including Peak Distortion Analysis (determines channel worst case bit pattern)

VerifEye (Statistical convolution approach)

Including 8b/10b with disparity algorithm





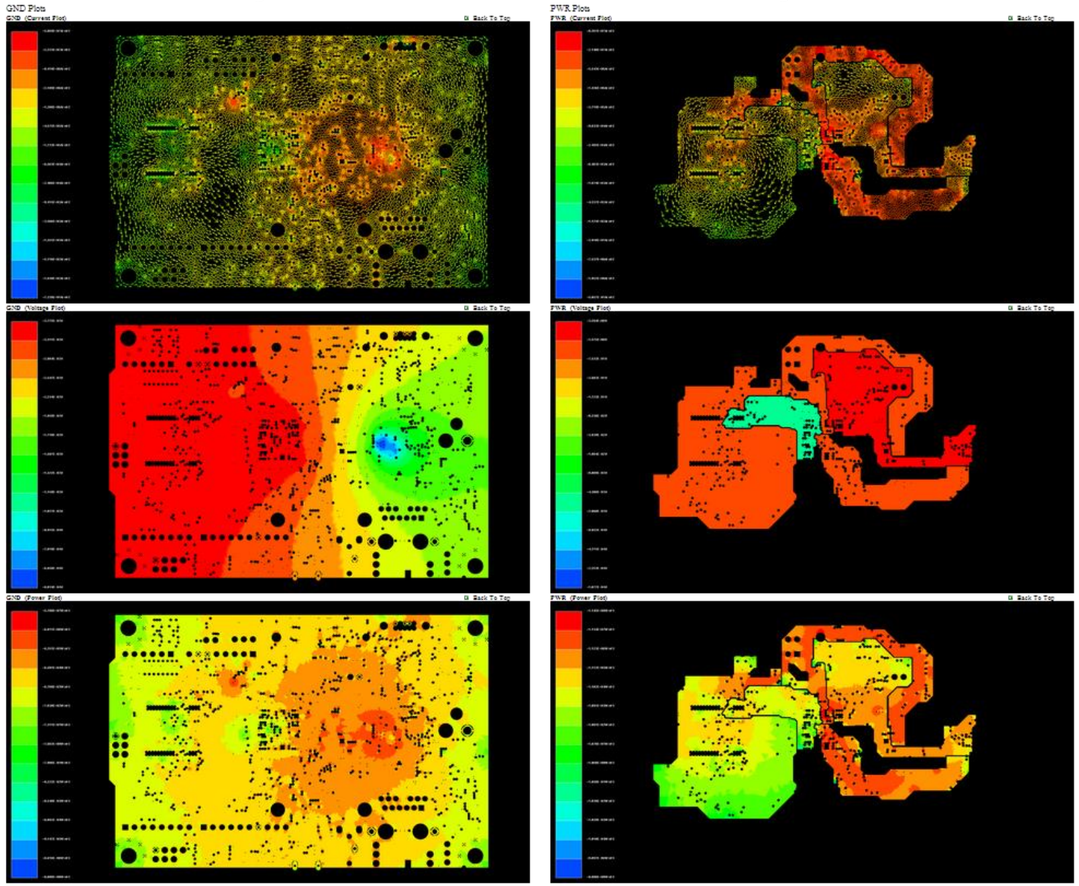
ANSYS SIwave——DC IR Drop Analysis

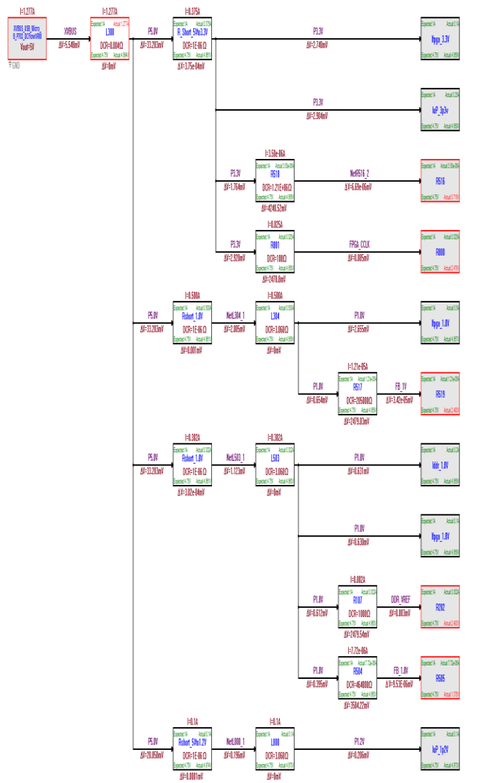
GND layer ***PWR Layer***

Current Plot

Voltage Plot

Power Plot

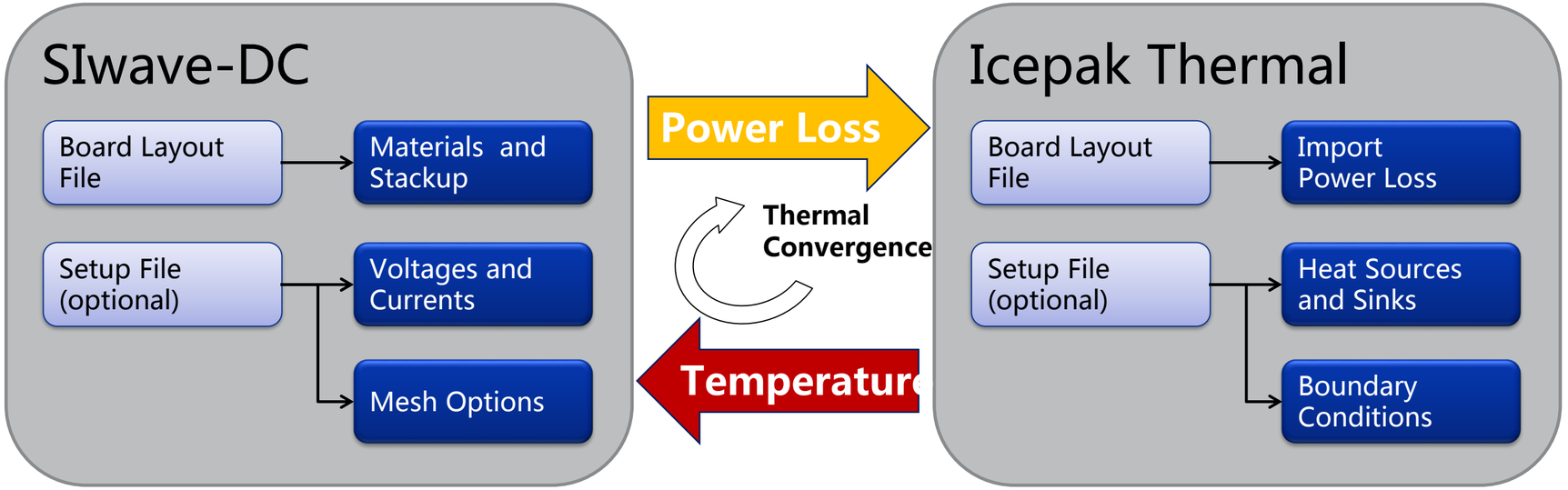


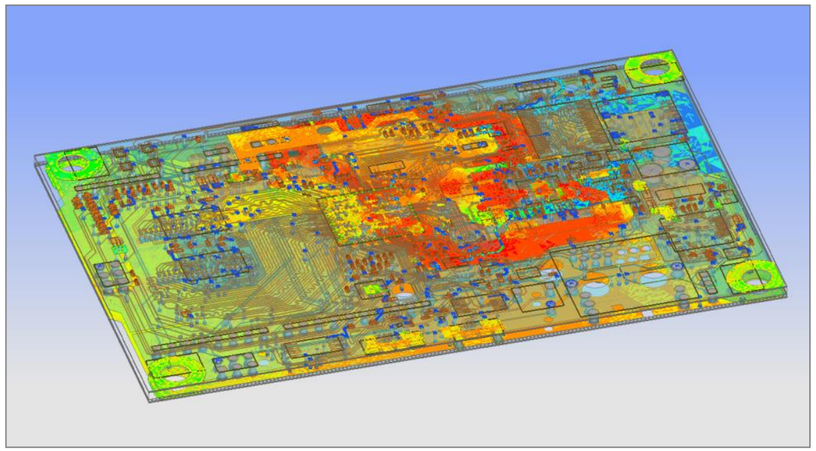


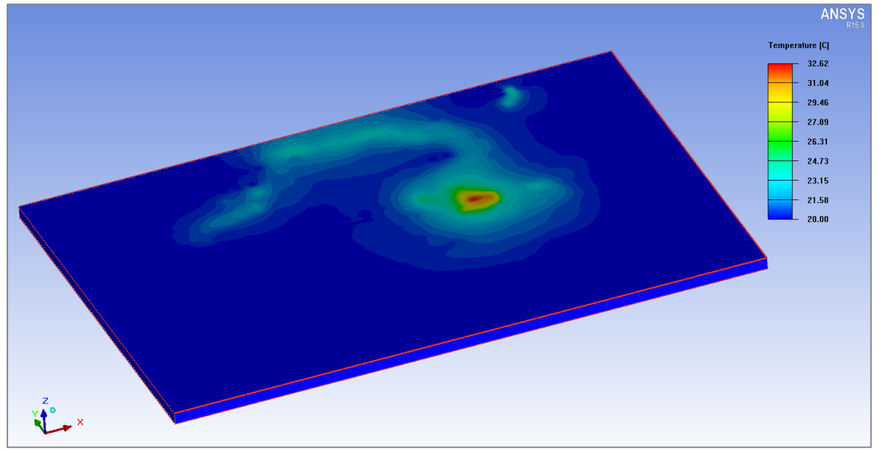
DC HTML Report

DC Power Tree (Signal Flow Graph)

ANSYS SIwave——Bi-directional Thermal Coupling with Icepak

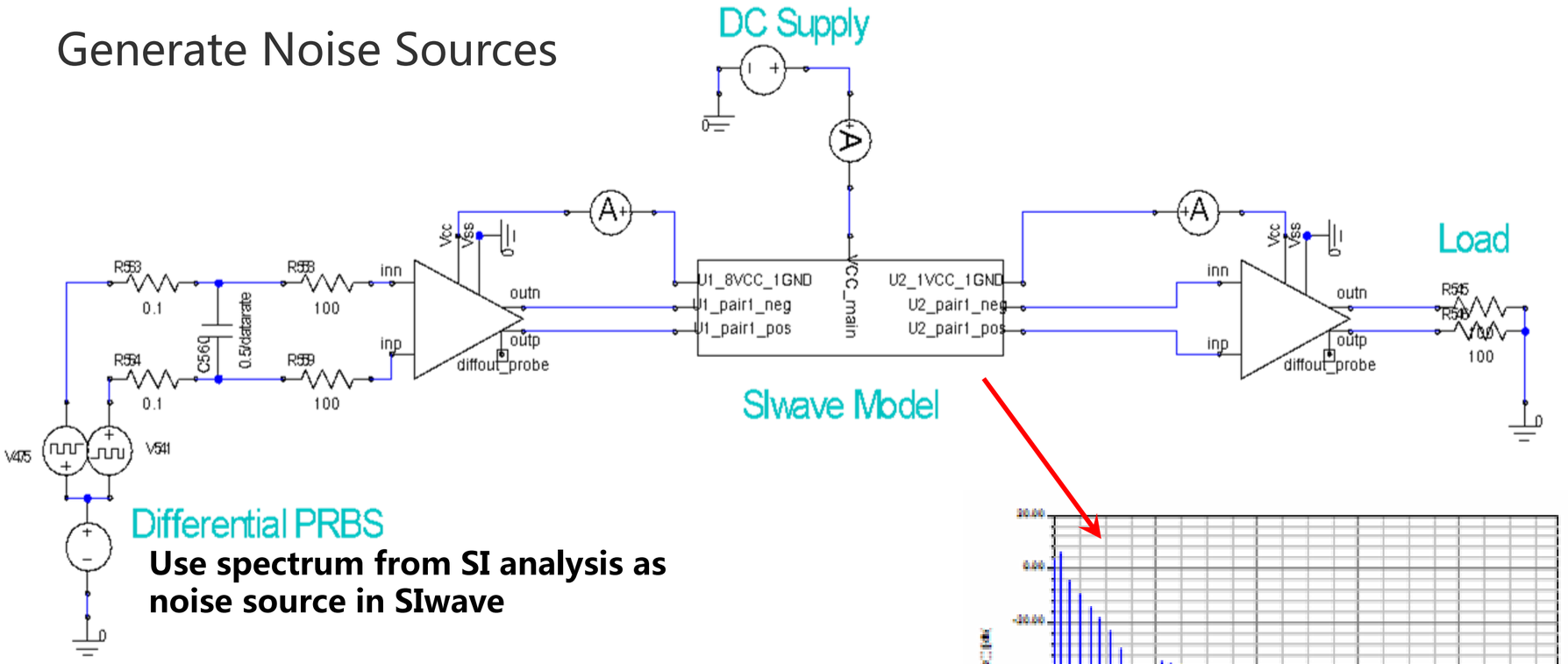




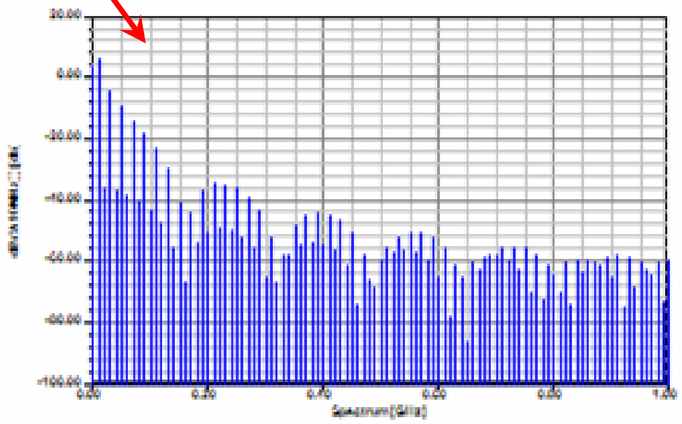


ANSYS SIwave——EMI/EMC

Generate Noise Sources

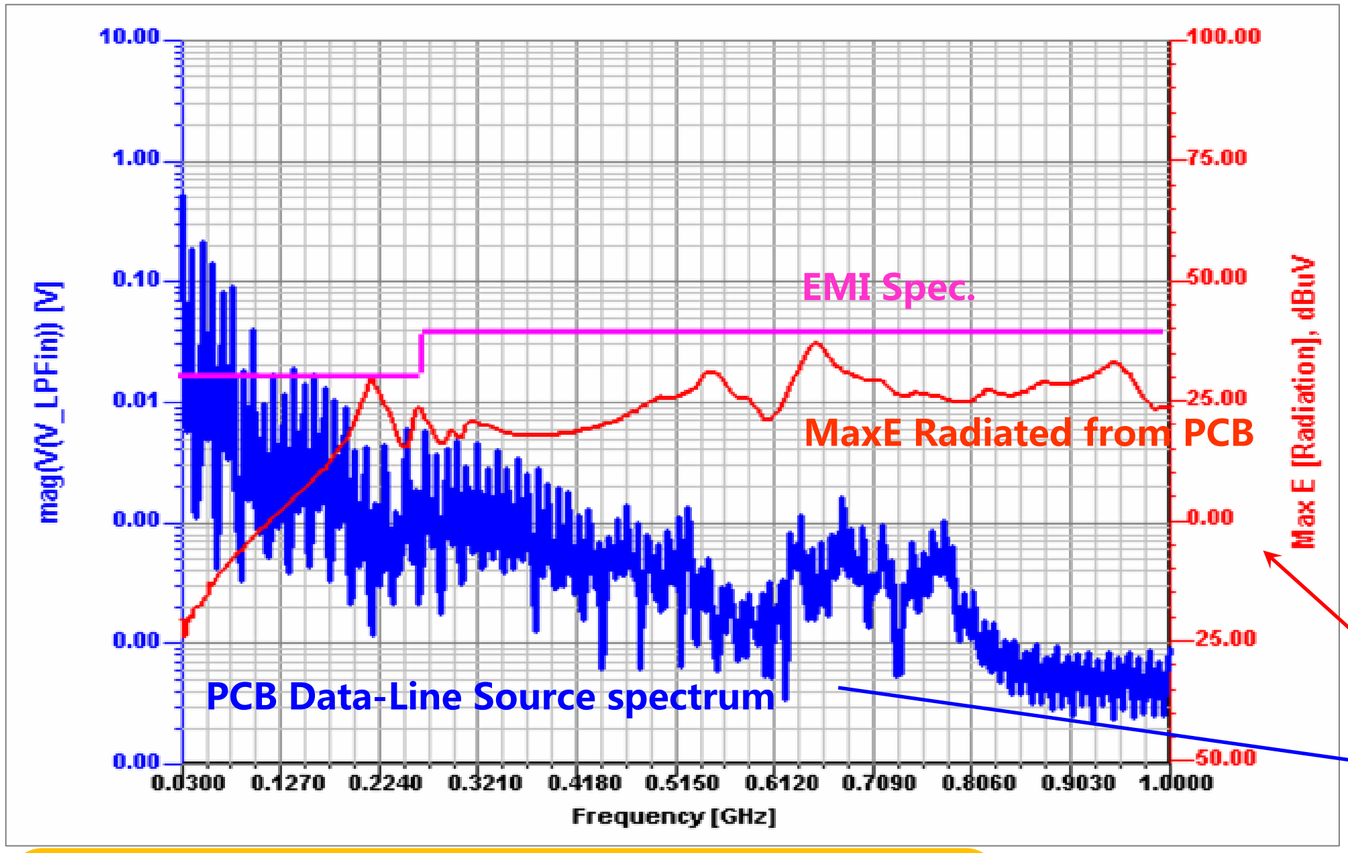


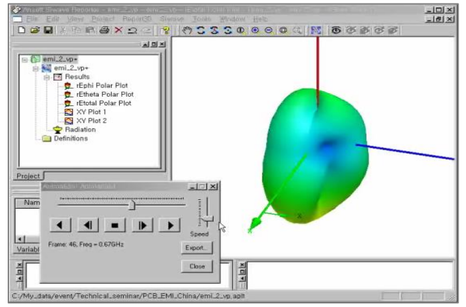
Use spectrum from SI analysis as noise source in SIwave

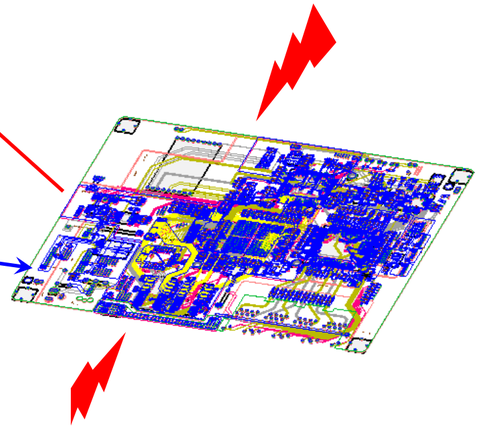


ANSYS SIwave——EMI/EMC

Plotting Far Fields







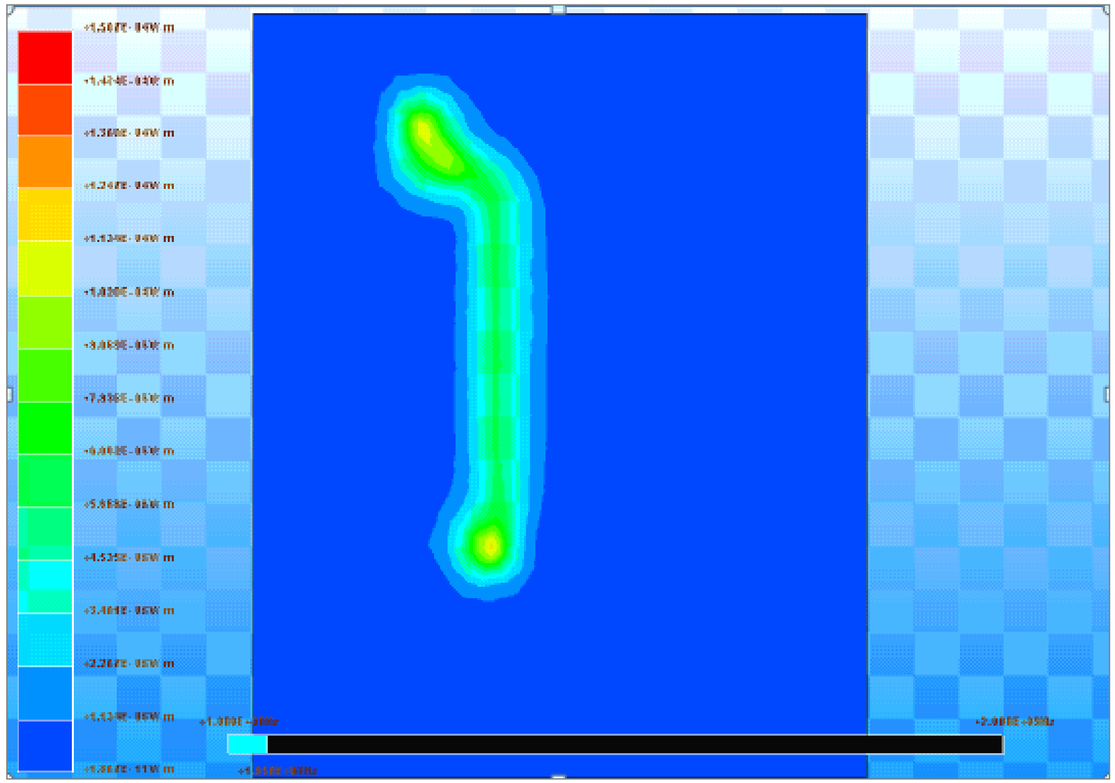
SIwave

ANSYS SIMULATION ADVANTAGES:

- **Fast and Accurate**
- **EMC Normative testing in few minutes**
- **No physical prototype and expensive anechoic chamber needed**

ANSYS SIwave——EMI/EMC

Near Field

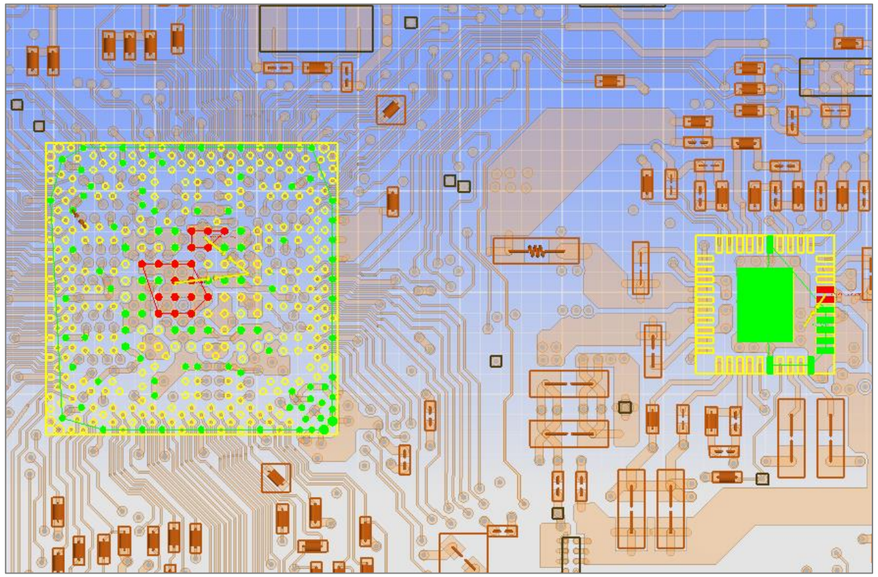


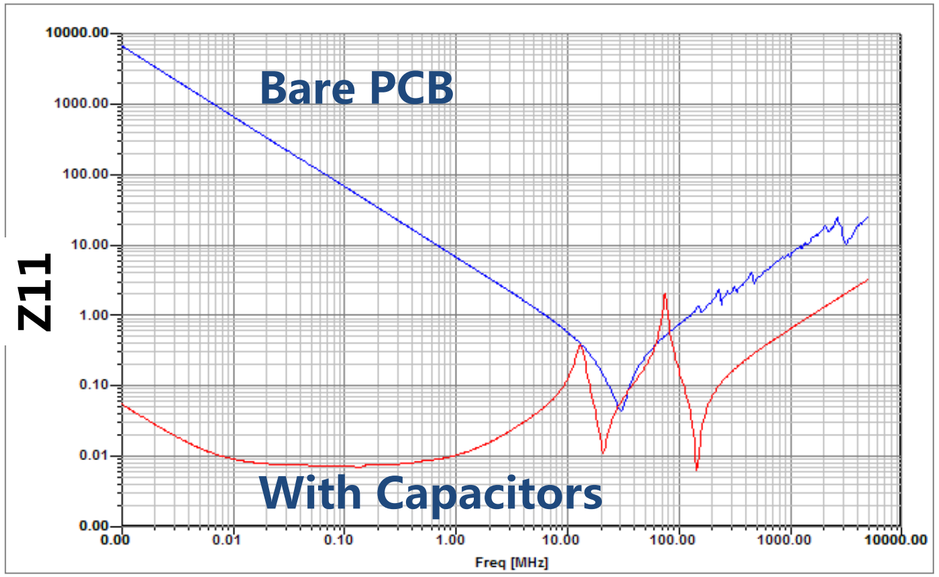
ANSYS SIMULATION ADVANTAGES:

- **Fast and Accurate**
- **Recognize critical areas on the PCB**
- **No physical prototype and expensive anechoic chamber needed**

ANSYS SIwave——Power Delivery Network Impedance

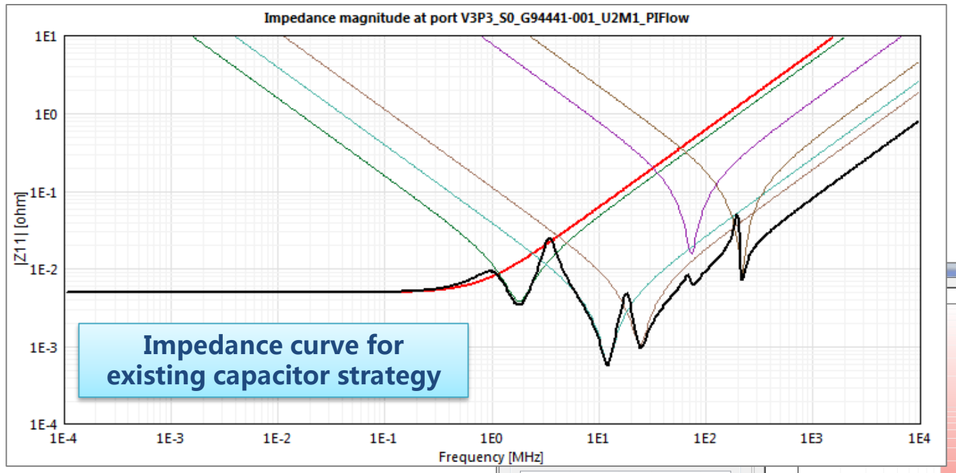
Full-wave extraction of entire PDN including:
- Board geometry
- Passive components

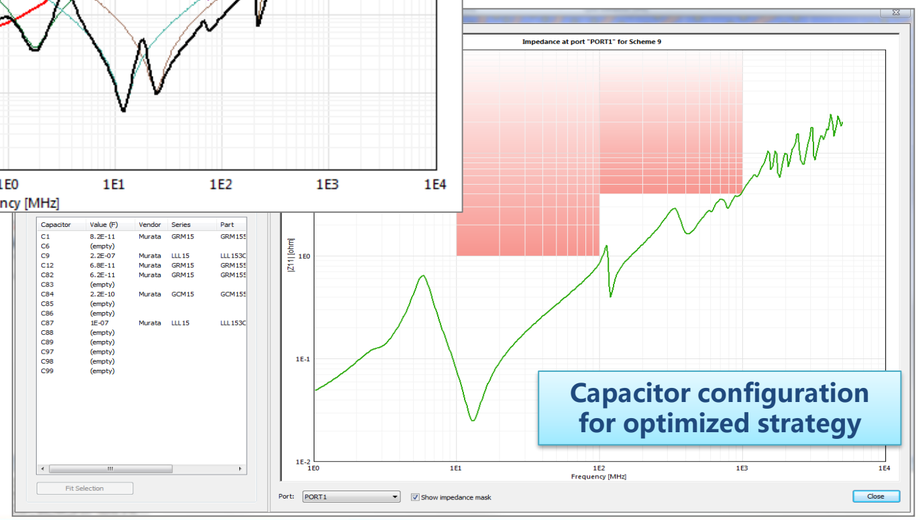


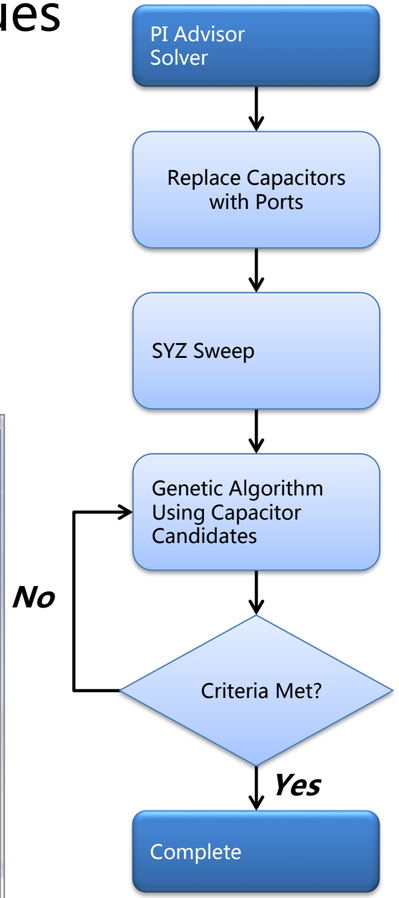


ANSYS SIwave——PI Advisor

- PI Advisor is an in-built tool that automatically optimizes De-coupling Capacitor Strategy for packages and boards
- Quick calculation for determining optimal capacitor values
- Optimization based on given impedance mask

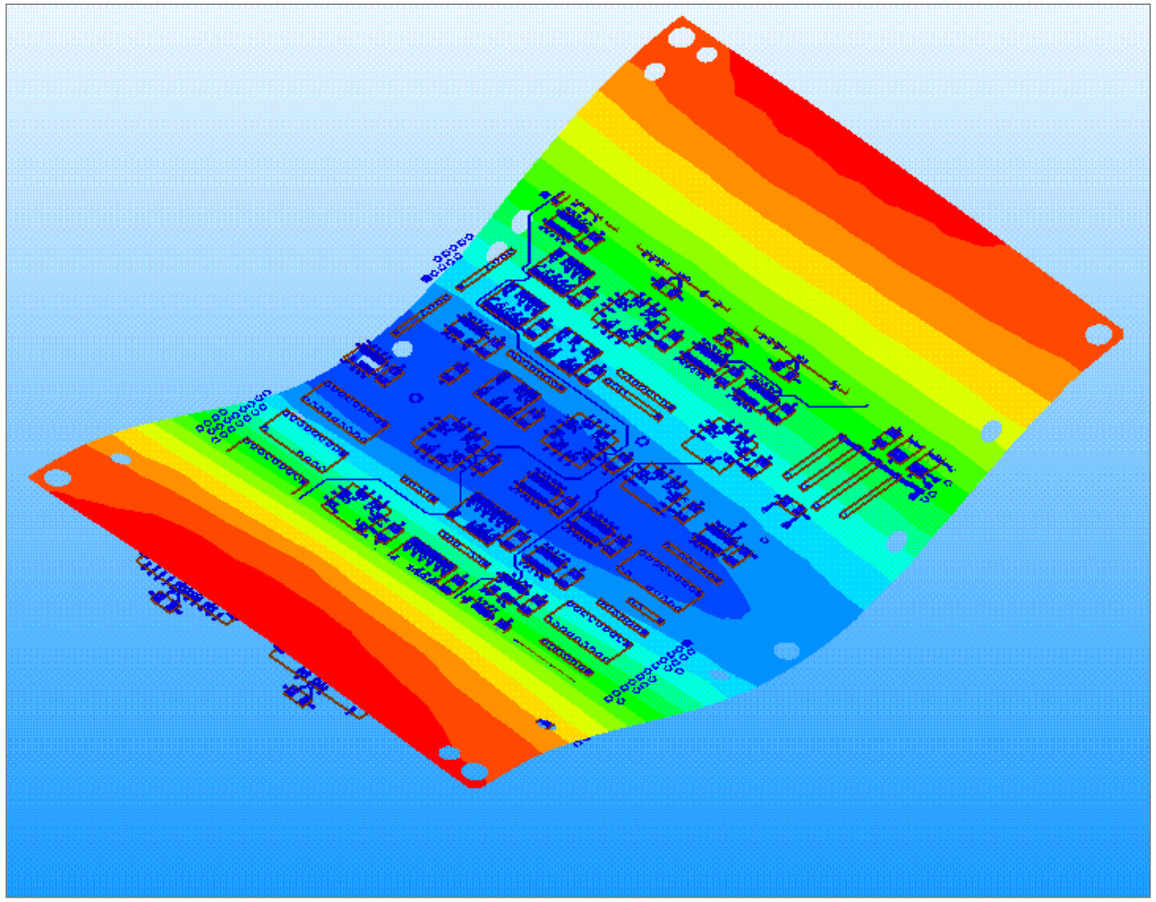






ANSYS SIwave——Resonant Modes

- **Resonant modes highlight potential problem areas of a PCB or Package**
- **Red and blue areas indicate high impedances at a particular frequency**



目录

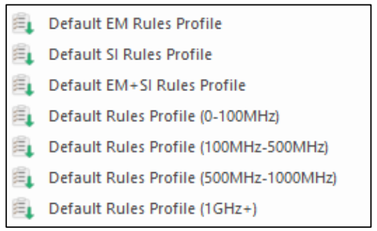
ANSYS SIwave新功能

- EMI Scanner –快速扫描整个设计，寻找可能导致EMI问题的违反规则的行为；
- Electromigration analysis电迁移分析 –利用电流和温度解析预测高风险MTTF区域；
- 改进了SIwave中的HFSS区域，允许分布式求解器和频率扫描，以及裁剪操作的清理；
- 层叠向导
- 背钻向导

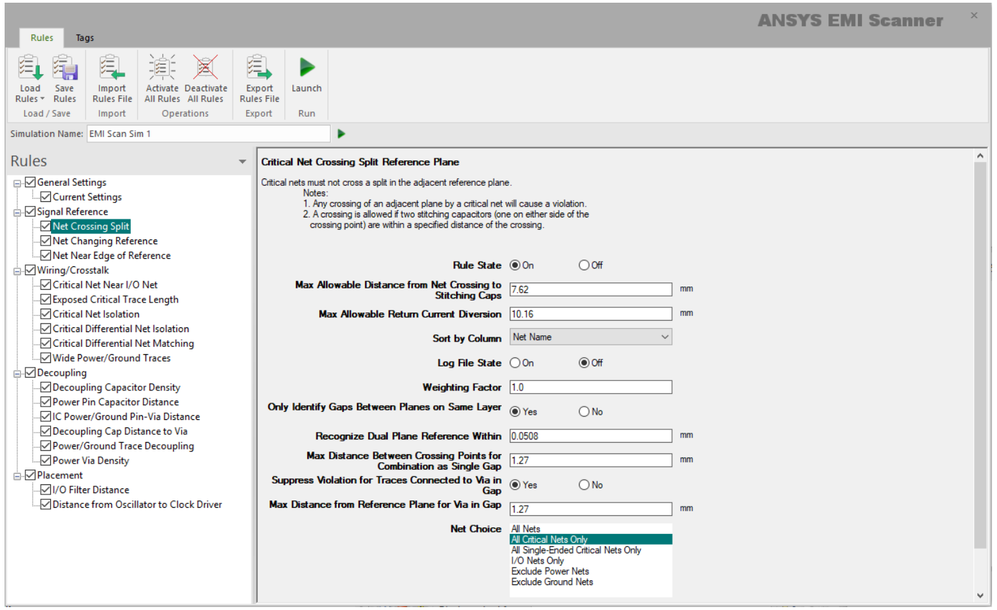
EMI Scanner – “ERC” EMI Rules Checker

Included With SIwave license &
Available within SIwave or 3D Layout Design

- 对可能导致EMI/EMC问题的常见布局违规行为的全板分析
- 可用于不同操作条件和频率范围的示例规则集



- 规则文件可以导出/导入到简单的xml文件中



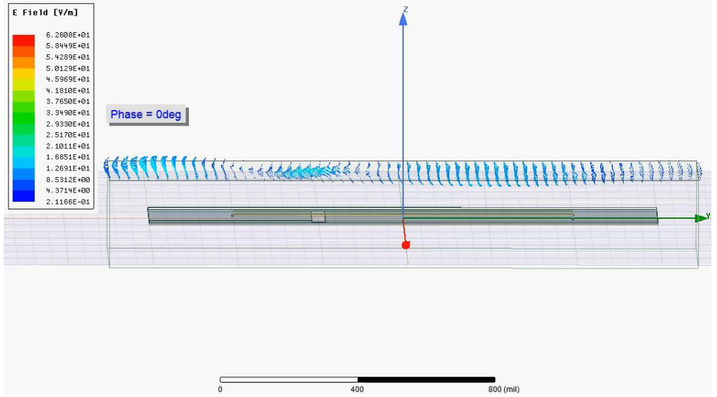

```
    </param>
    <param label="Recognize Dual Plane Reference Within" name="ALLOW DIST VARIATION" type="float
      <description>Instructs EMI Scannner to consider both planes as a reference when checking
      <value type="default">0.0508</value>
    </param>
    <param label="Net Choice" name="NET LISTING" type="single_select_list" view="advanced">
      <description>Specifies the type of Nets to include in this rule analysis.</description>
      <value altvalue="ALL">All Nets</value>
      <value altvalue="CRITICAL" type="default">All Critical Nets Only</value>
      <value altvalue="SINGLE_CRITICAL">All Single-Ended Critical Nets Only</value>
      <value altvalue="IO">I/O Nets Only</value>
    </param>
  </rule>
</ruletype>
```

通过在设计过程的早期提供洞察力，显着地减少了对EMI遵从性的验证

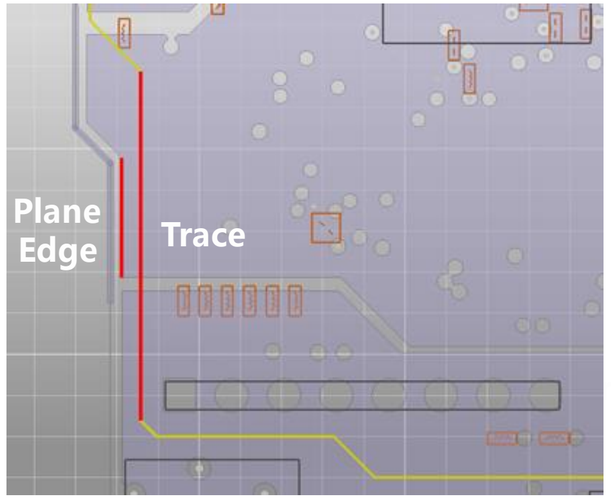
电磁干扰规则

- Signal Reference
  - Net Crossing Split
  - Net Changing Reference
  - Net Near Edge of Reference
- Wiring/ Crosstalk
  - Critical Net Near I/O Net
  - Exposed Critical Trace Length
  - Critical Net Isolation
  - Critical Differential Net Matching
- Placement
  - I/O Filter Distance
  - Distance from Oscillator to Clock Driver

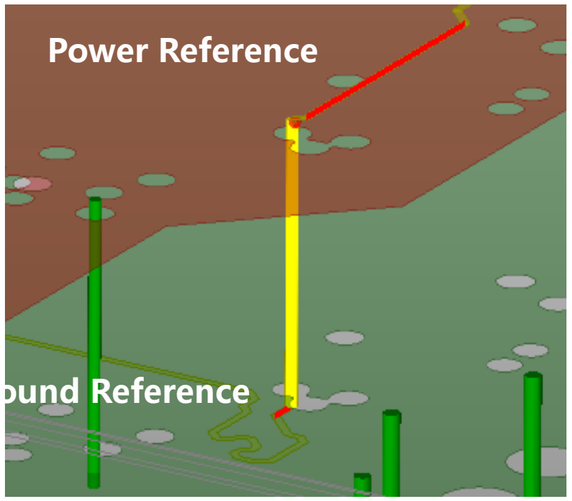
Net Crossing Split



Net Near Edge of Reference



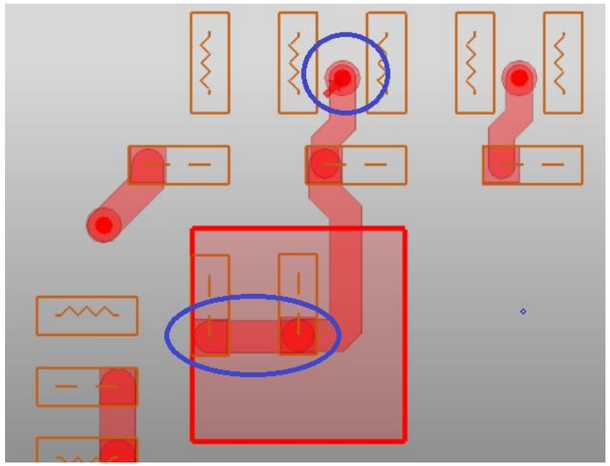
Net Changing Reference



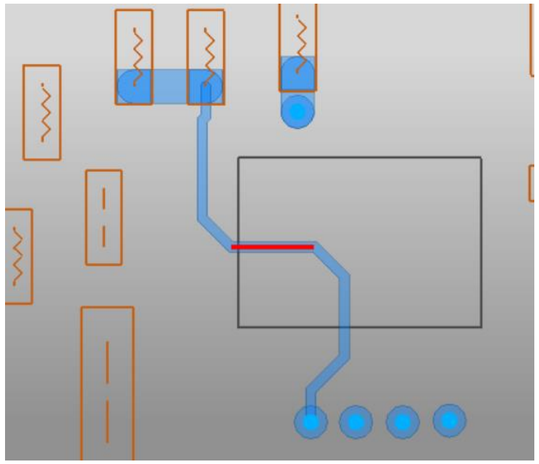
电源完整性规则

- Wiring
  - Wide Power/Ground Traces
- Decoupling
  - Decoupling Capacitor Density
  - Power Pin to Capacitor Distance
  - IC Power/Ground Pin to Via Distance
  - Decoupling Cap Distance to Via
  - Power/Ground Trace Decoupling
  - Power Via Density

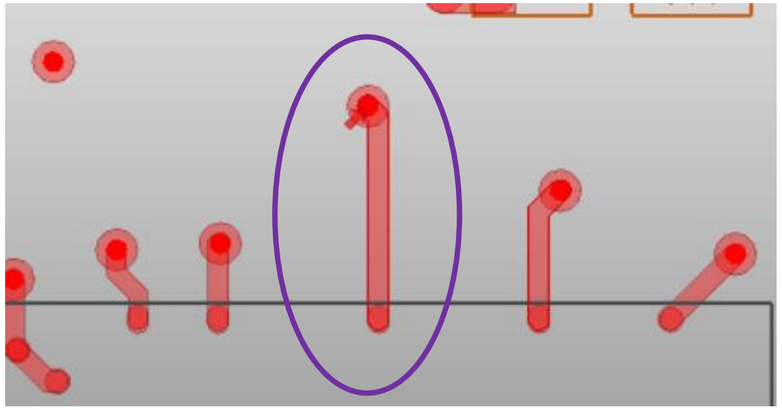
Decoupling Capacitor Distance to Via



Wide Power/Ground Trace Check



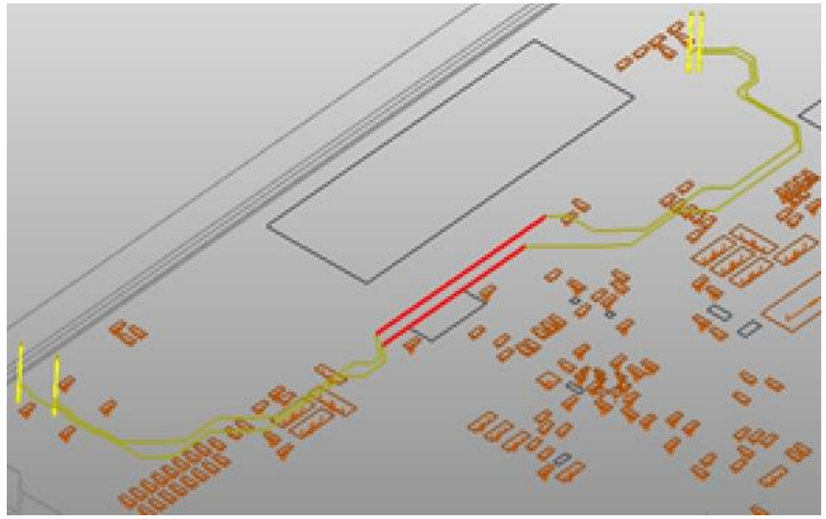
IC Power Pin to Via Distance



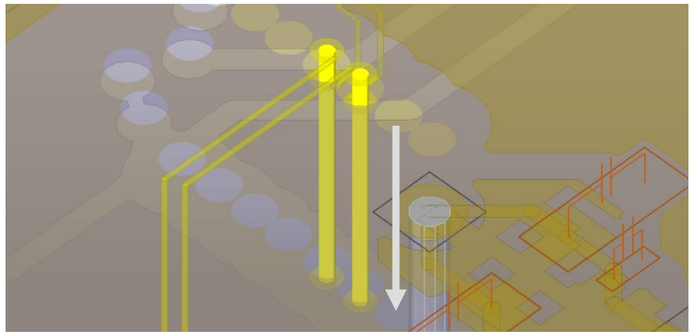
网络和过孔完整性规则

- Net Integrity
  - Net to Net Coupling
  - Net Stubs
  - Net Crossing Split
  - Critical Net routing between Reference Planes
  - Diff Pair Running Skew
- Via Integrity
  - Via to Net Coupling
  - Via Stub Length

Net to Net Coupling



Via Stub Length

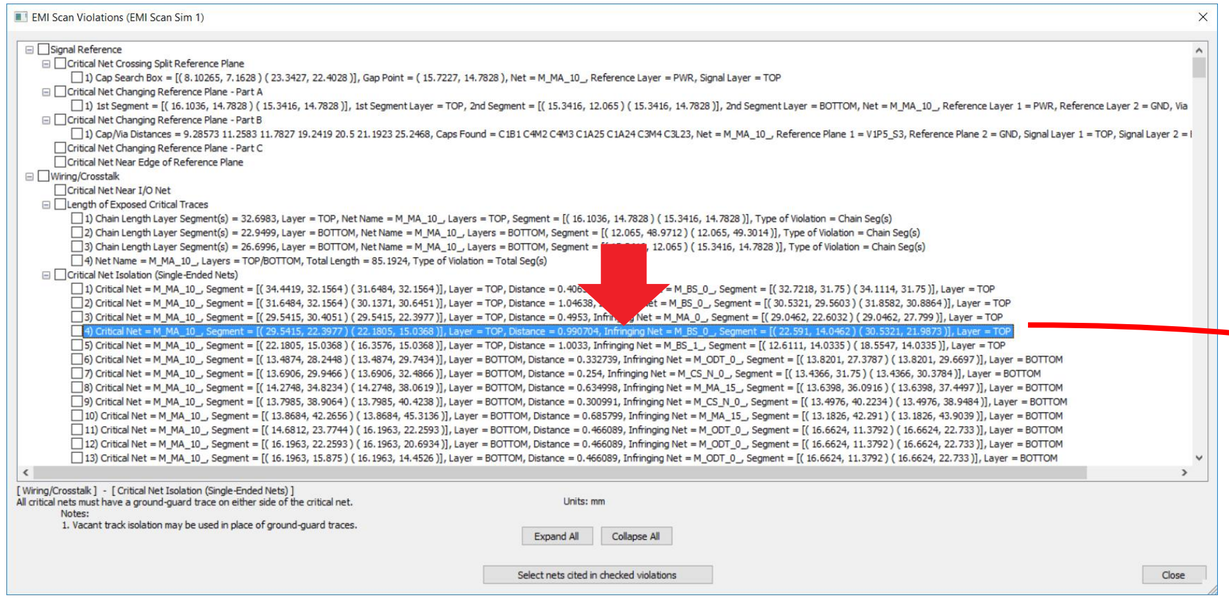


EMI扫描输出

Included With SIwave license &
Available within SIwave or 3D Layout Design

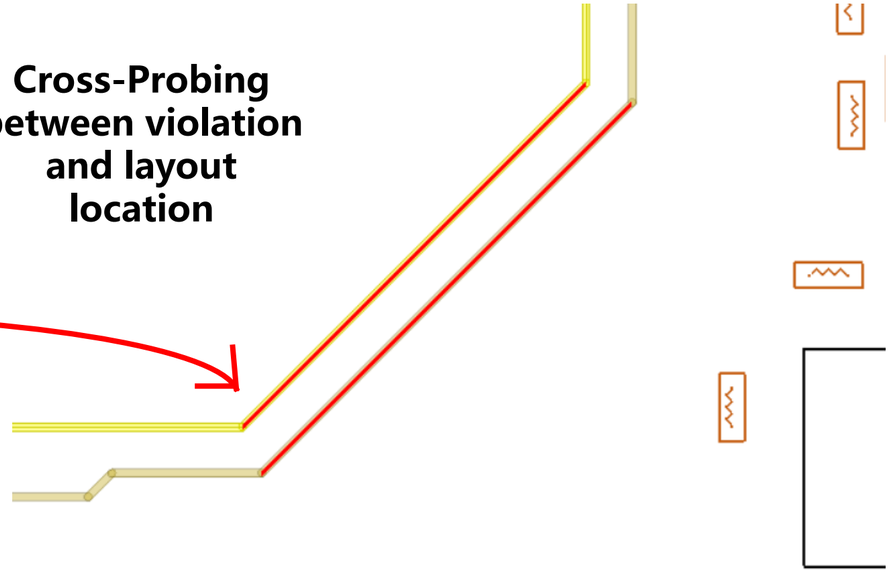
- 违规行为按类型显示
- 在列表中选择冲突高亮显示布局中的违规位置

Violation List



Layout View

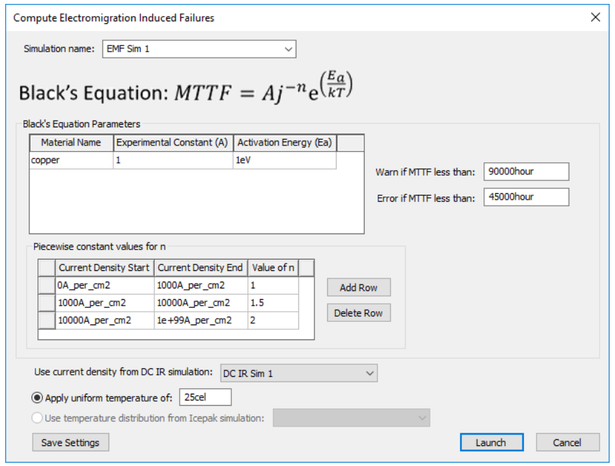
Cross-Probing between violation and layout location

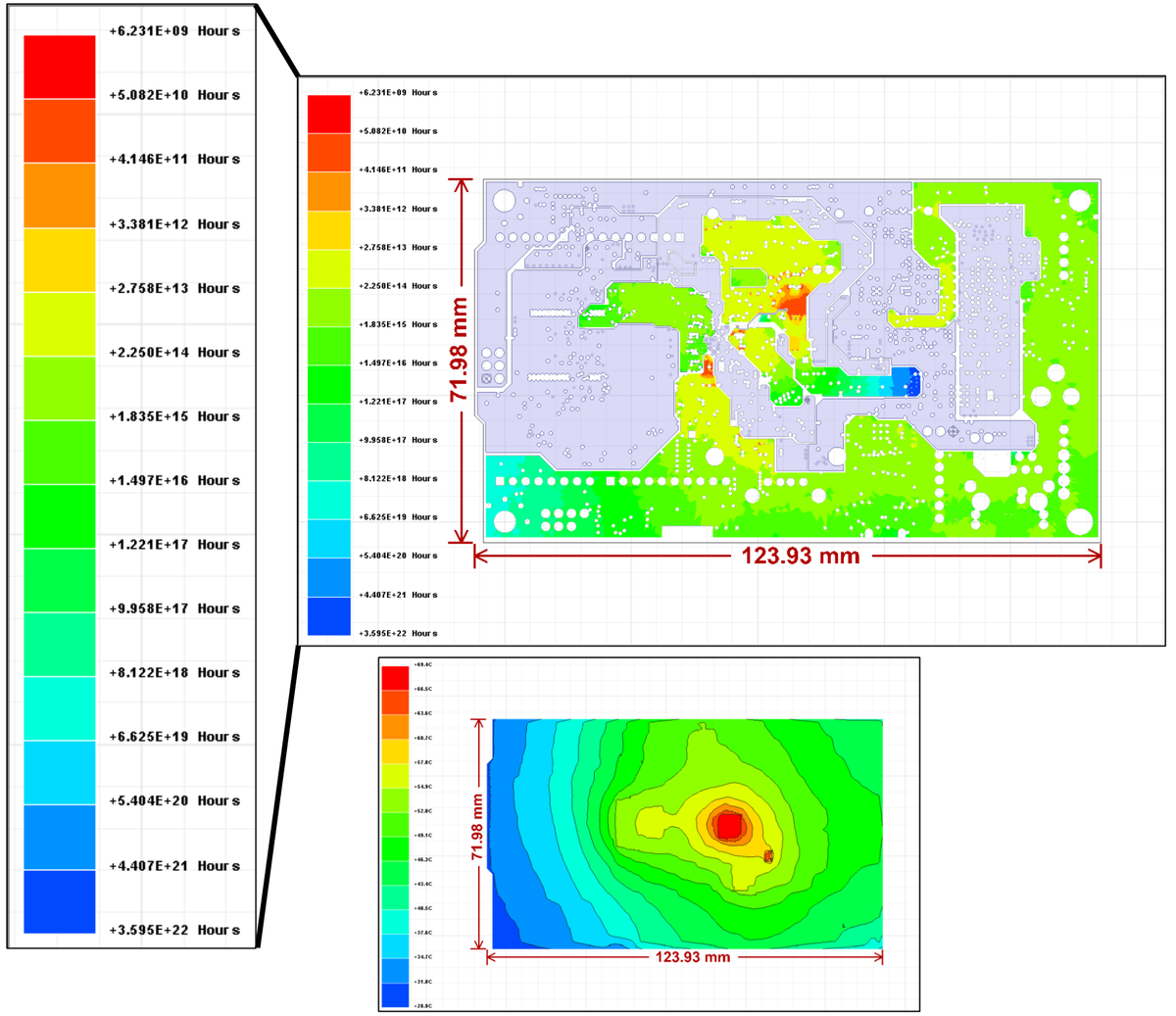


电迁移分析

Included With SIwave license

- 使用Black方程预测平均失效时间(MTTF)，突出潜在关注区域
- 需要直流压降仿真
- 也可以通过包含Icepak结果来包括温度效应

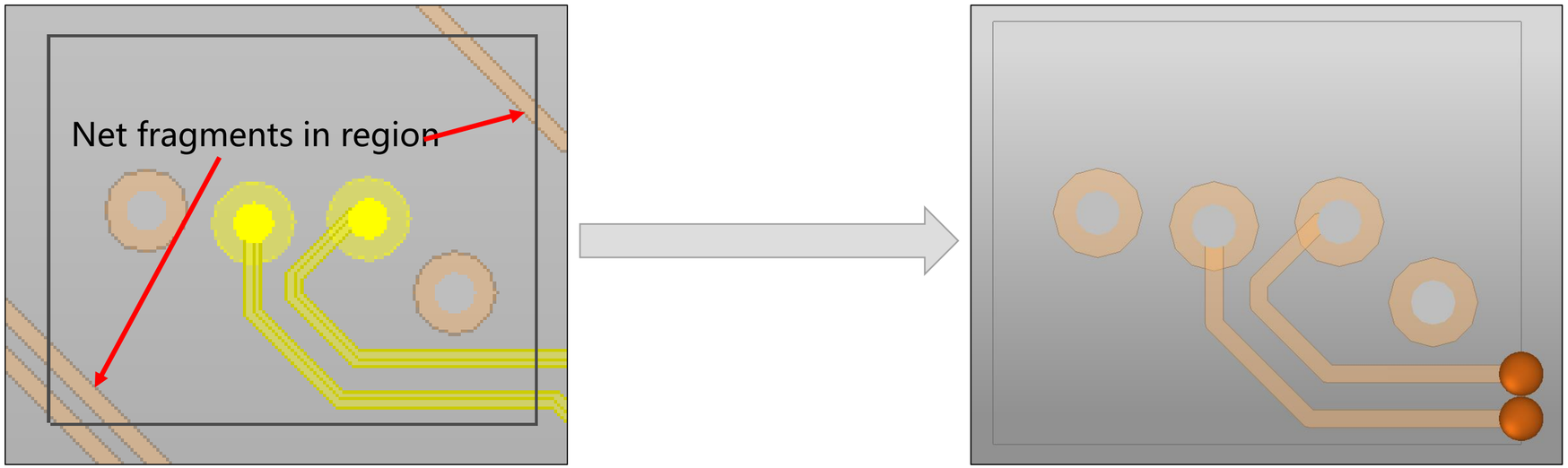




HFSS Regions in SIwave

- Released in R19.1
- 2019 R1增强
  - 每个区域的并行化频率扫描
    - 区域串联求解
  - 与独立分布式程序或调度程序兼容
  - 清理个别区域

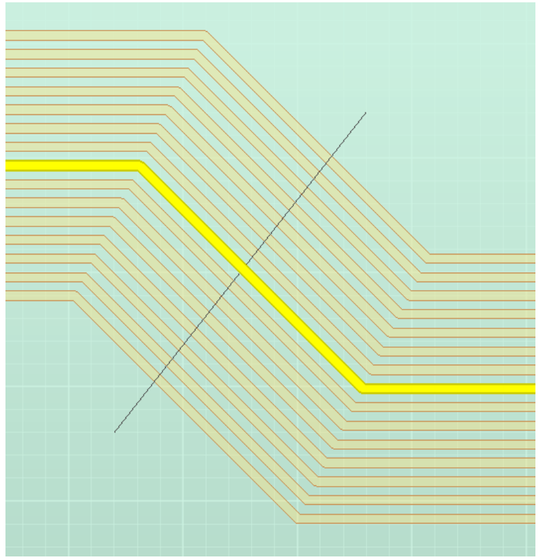
Net fragments eliminated for HFSS
- Reduced mesh / solve time for region

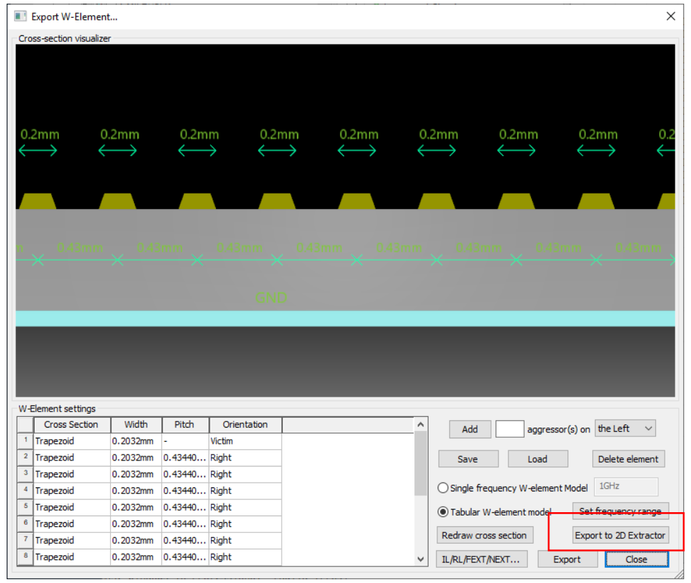


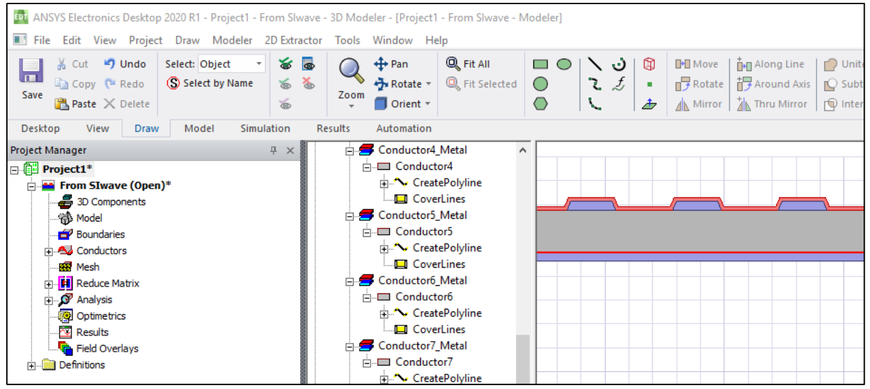
Stackup Wizard Enhancements - W-element Analysis

- Draw polyline which crosses traces in layout to populate W-element export dialog
- Export W-element as well as 2D Extractor project

Select “victim” trace

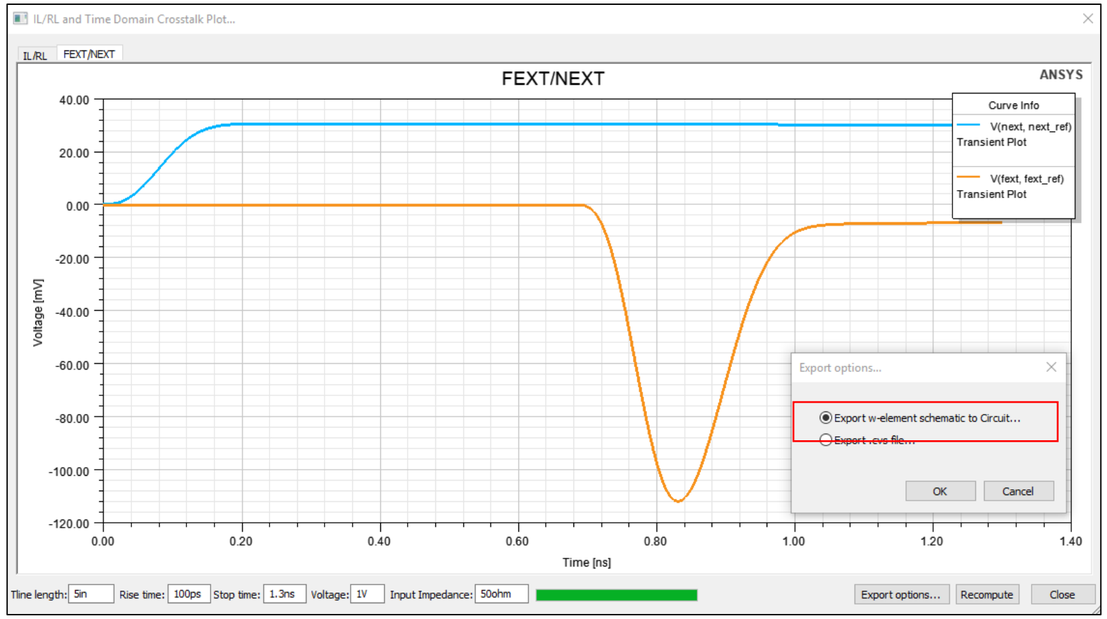


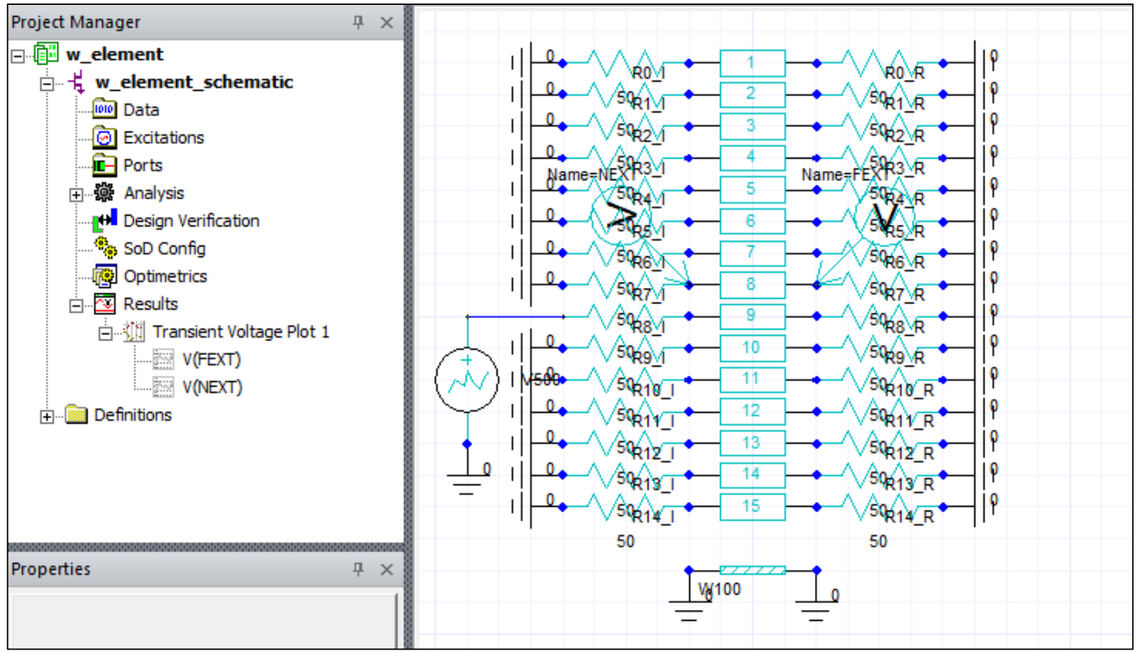




Stackup Wizard Enhancements

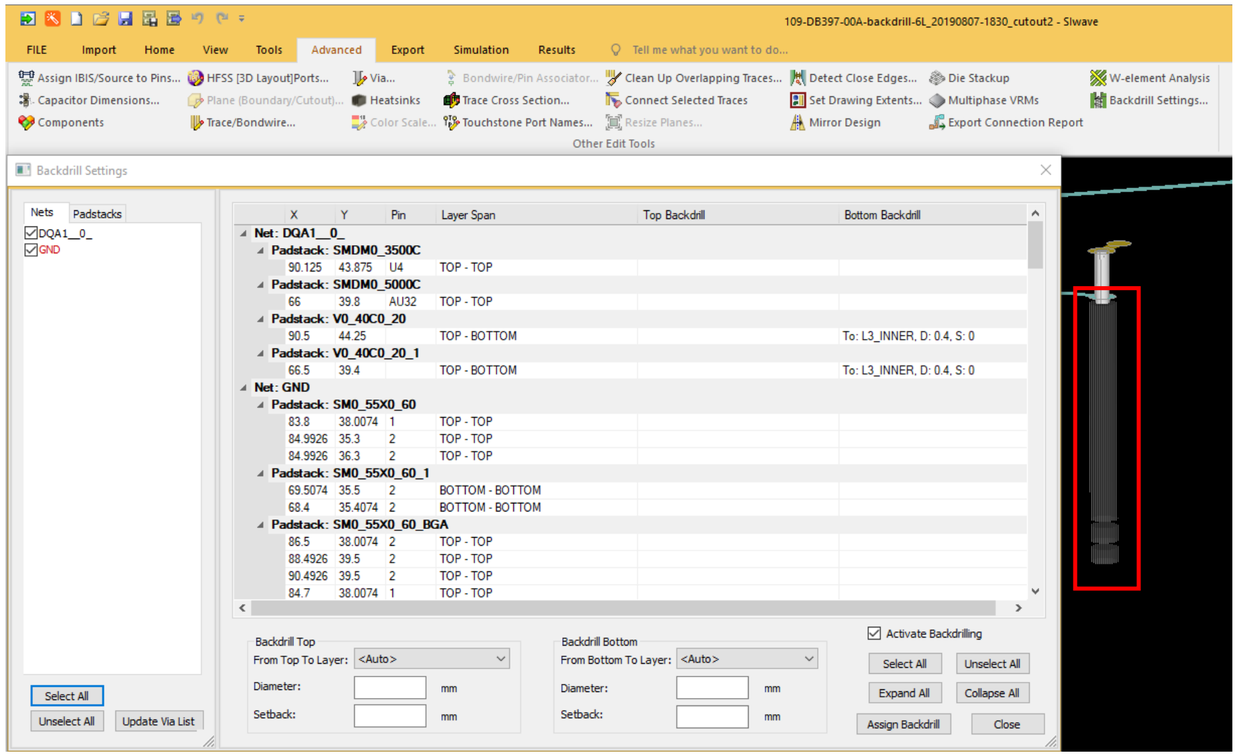
- Export preconfigured schematics to AEDT for detailed IL/RL and FEXT/NEXT sims

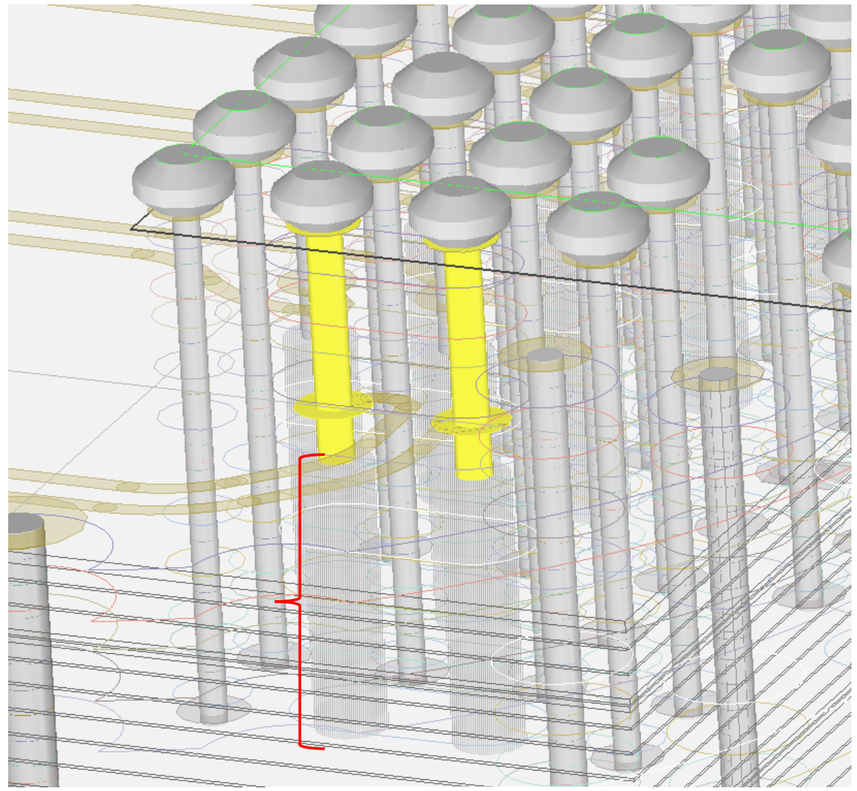




Via Backdrill Configuration UI

- Backdrill information imported from ODB++ and 3D Layout
- Support for setback distances



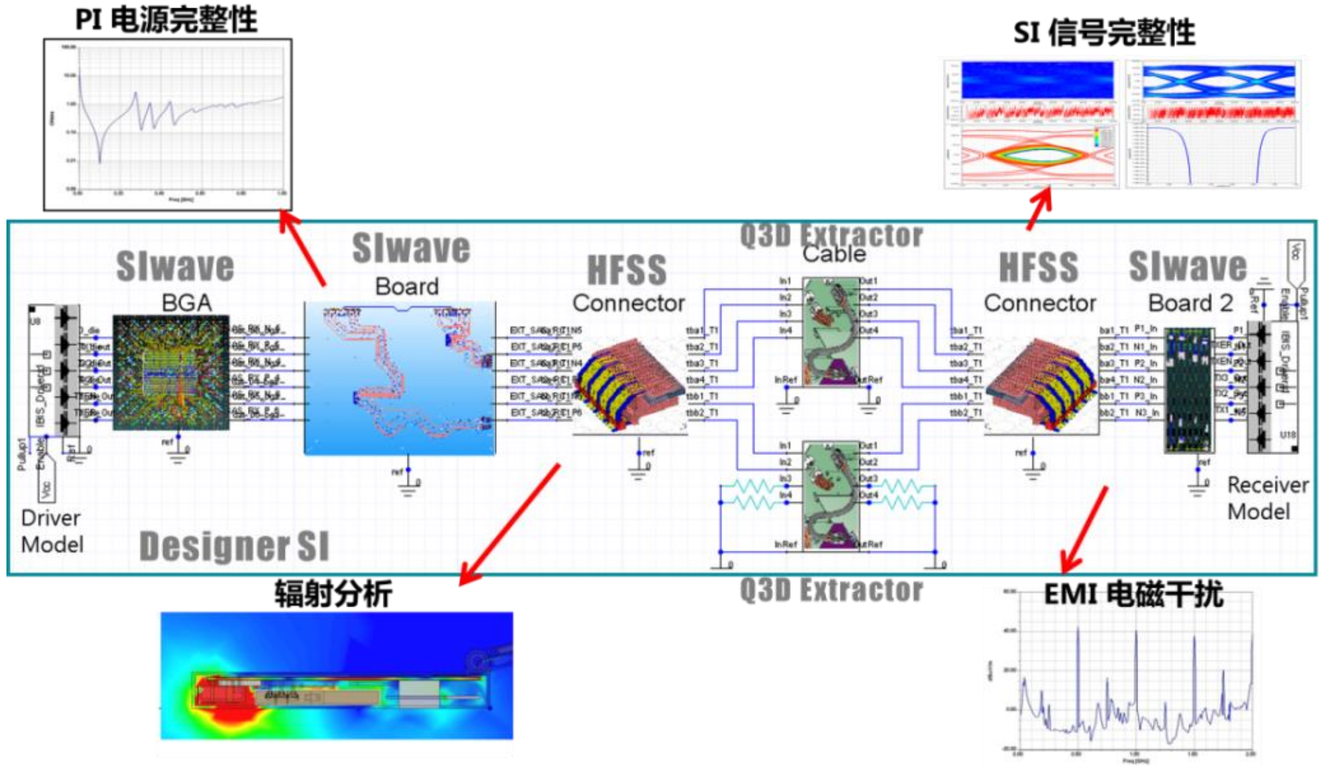


Vias stub drilled out

小结

随着通信技术的发展，及对信号传输速率的要求飞速提升，电子产品设计要求越来越苛刻，创新产品设计越来越依赖于高频电磁场仿真。

在这一领域，ANSYS凭借强大的电磁场仿真平台，多个仿真器的综合应用，加速了电子产品的研发进程。



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期待与您的进一步合作 ☺

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