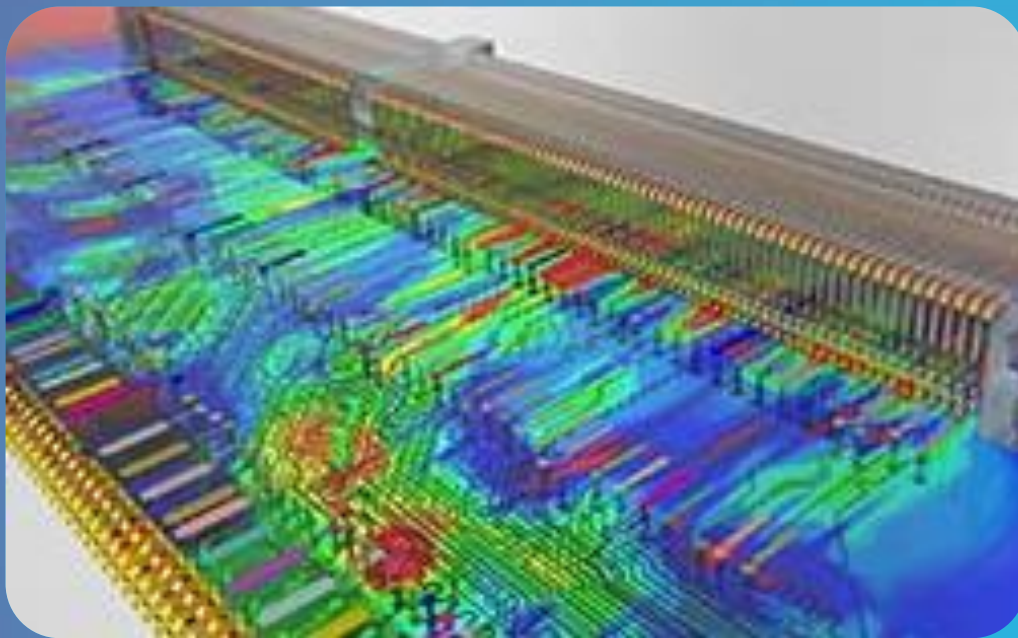




Ansys 2020 R2 EBU高频特性更新

艾迪捷信息科技（上海）有限公司

IDAJ-CHINA

高频电磁场技术经理 刘捷

Ansys 2020 R2 高频电磁场更新特性

Ansys 2020 R2在以下方面有新的提升：精简的电子工作流，热机械集成和高性能计算的提升。

- Ansys HFSS自动计算5G设备的生物兼容性，包括增强的用于阵列天线的HPC 3D组件DDM求解器。
- Ansys EMA3D电缆仿真工具提供平台级EMI/EMC电缆线束分析。
- Ansys SIwave自动报告信号完整性度量，并生成复杂的算法模型来确认系统性能，以供IC供应商选择。
- Ansys Icepak支持基于系统温度的动态热管理以自动保护有源器件特性。



High Frequency Electromagnetics

关键更新点

HFSS 3D

- 阵列天线3D组件: 直接矩阵求解选项
- 5G标准工具包
- 多动作自动分解计算, 带点粒子可视化
- HFSS SBR+: 近场分析及场图叠加
- Layered impedance边界条件支持复杂材料
- 改进分布式内存矩阵求解器的性能
- IE区域间的导体介质接触(Beta)

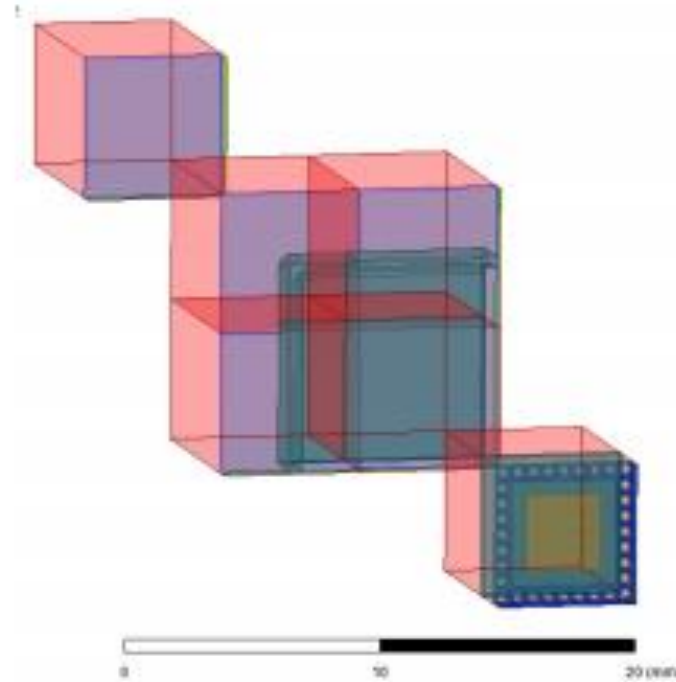
HFSS 3D Layout

- 支持HFSS 3D Components
- 具有Fast仿真模式的HFSS Auto-solution设置
- 基于GDS的设计: 改进工作流程和能力
- 通过netlist或电路图定义电路元件
- HFSS自动增强性能
- 基于点的RLC电路元件

Circuit

- SPISim: IEEE 803.3 COM and USB合规检查
- SPISim: IBIS-AMI模型生成和检查
- 频域结果报表创建改进
- 改进的直流和瞬态收敛阻尼算法
- EMIT工作流程和可用性改进

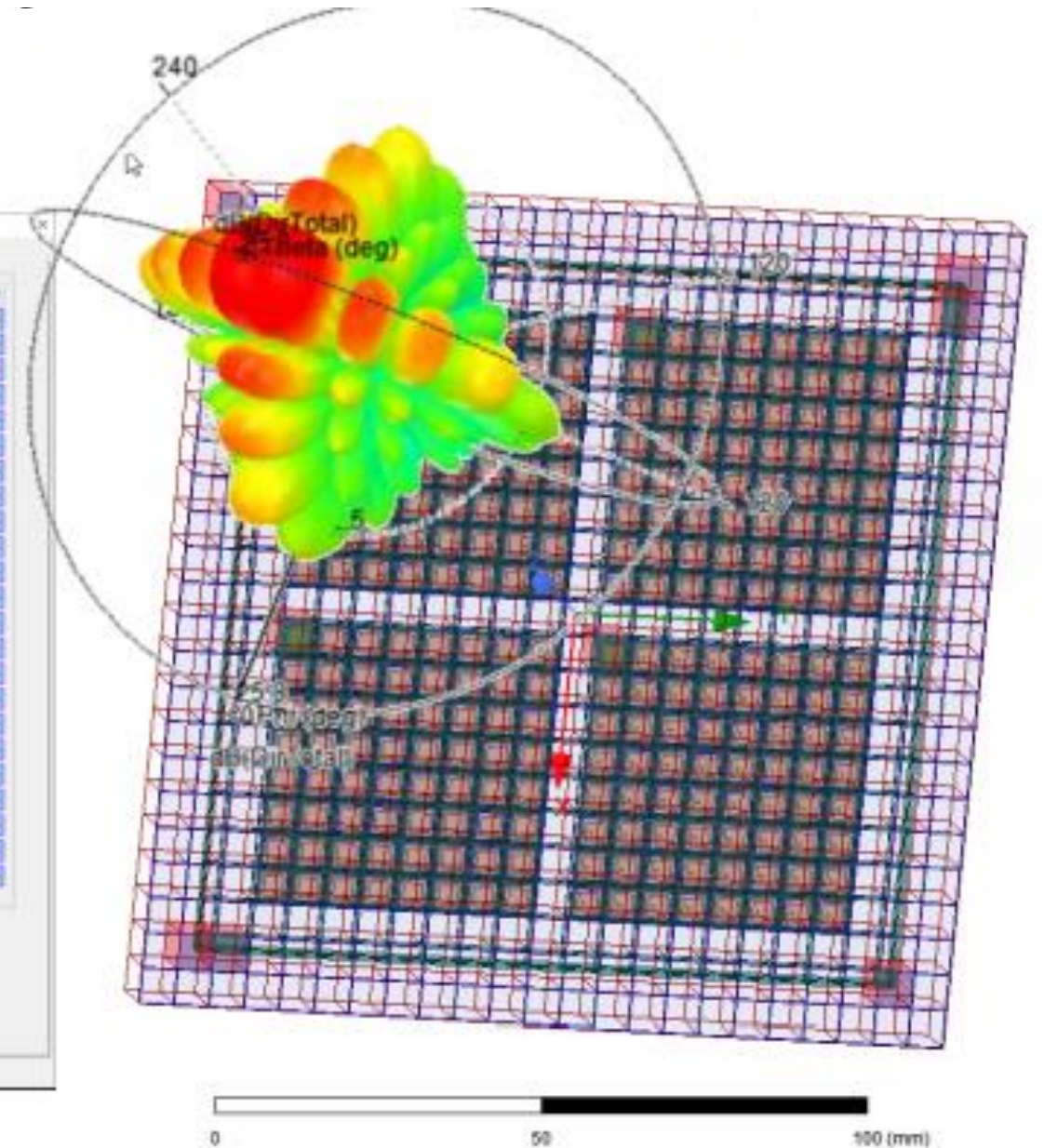
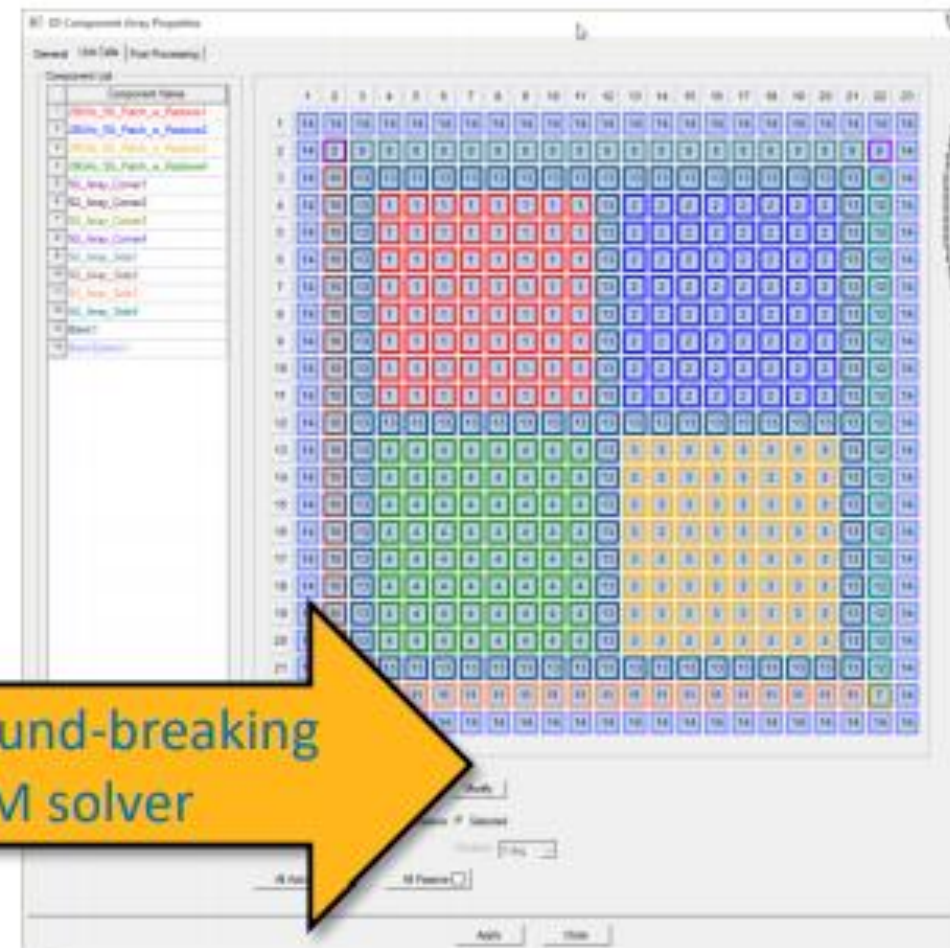
直接矩阵求解选项：改进相控阵天线分析



3D Comp Array

- Fast, concurrent adaptive meshing of unit cells
- Direct matrix solver effective in weakly coupled and large port count models
- Finite size effects, multiple elements including dummy element type(s)

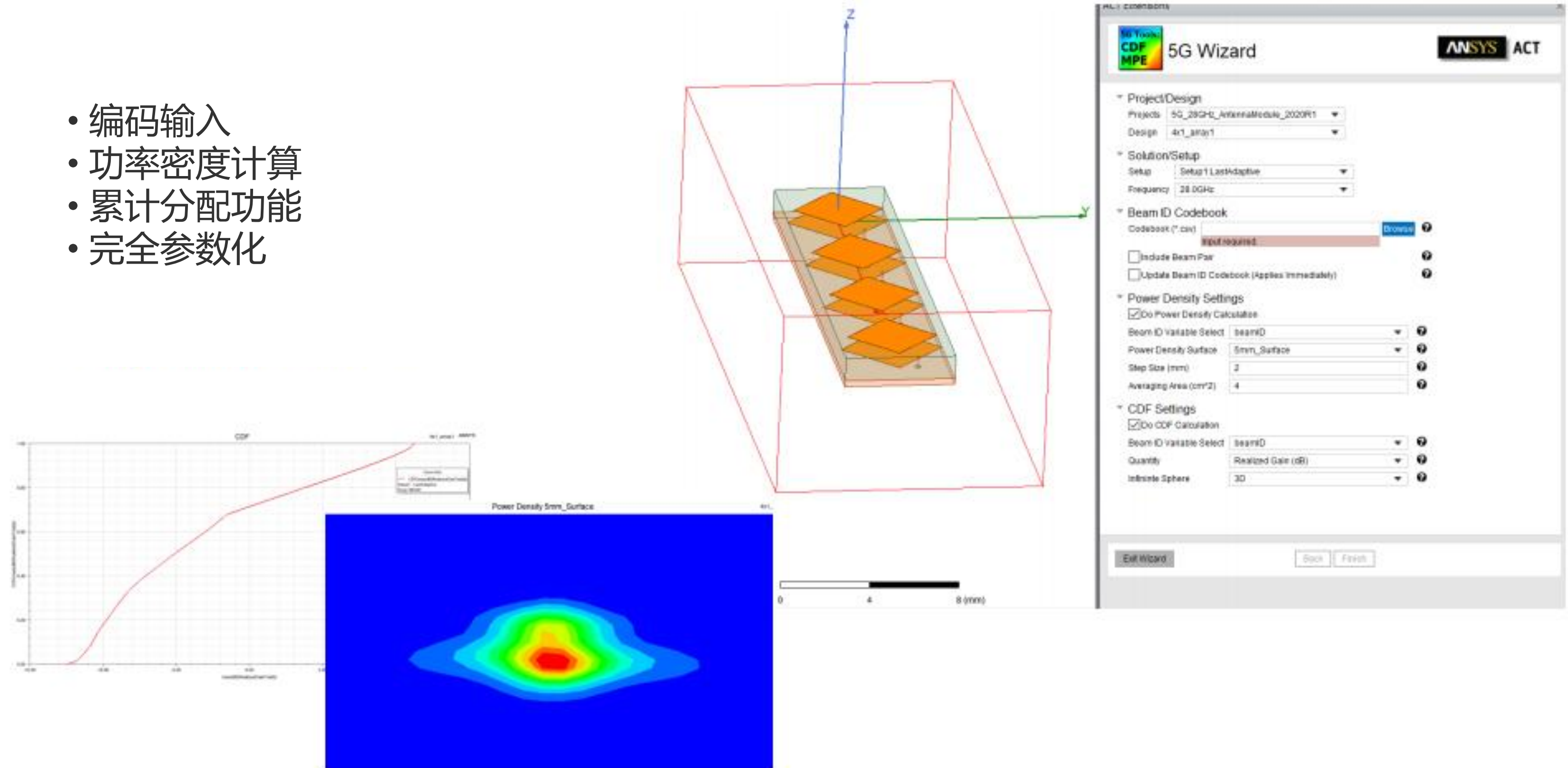
Built upon ground-breaking
HFSS DDM solver



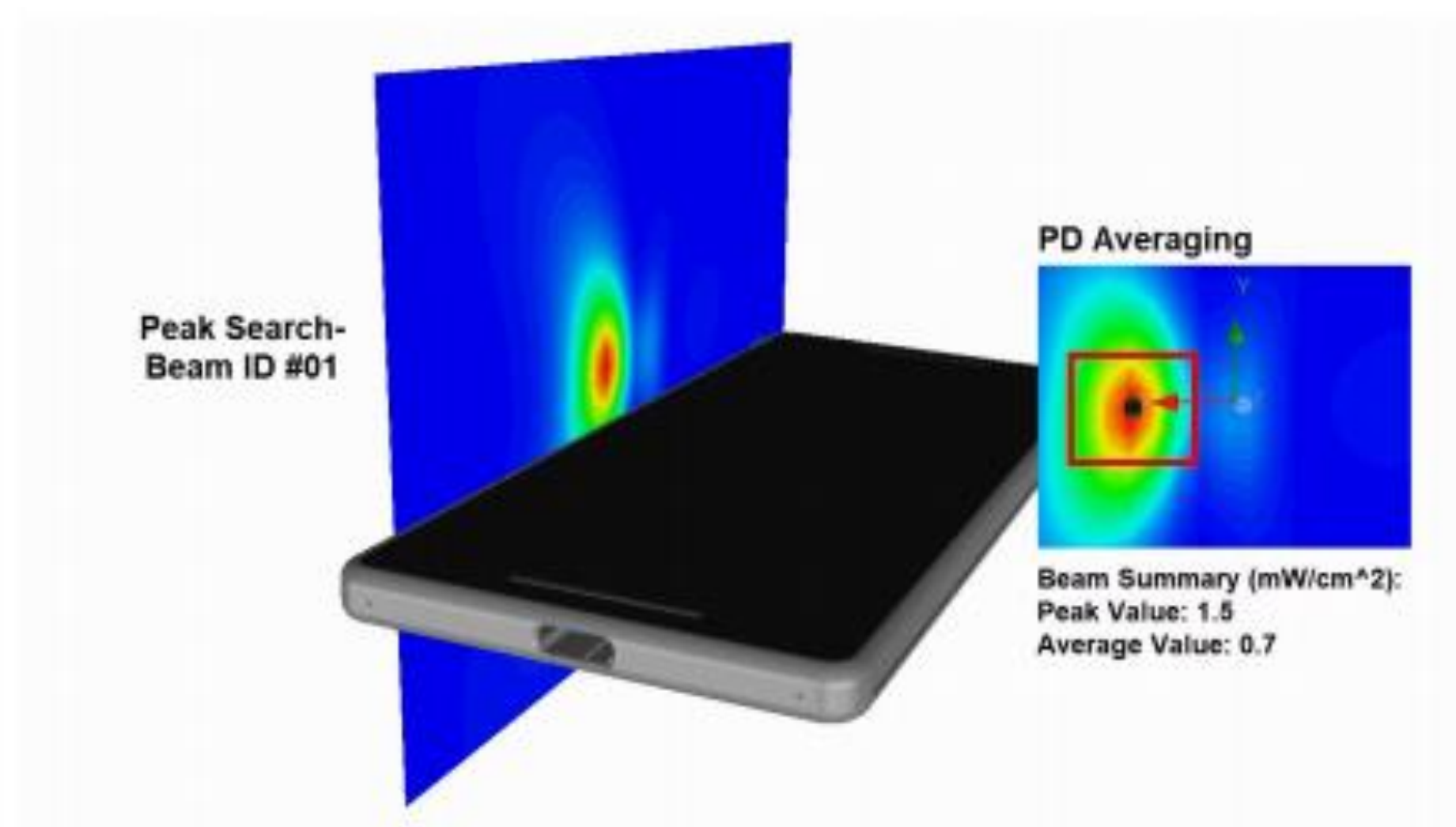
- Ansys 2020 R2：用直接矩阵求解器求解DDM阵列矩阵的选项
- 没有“阵列近似”
- 特别适用于5G毫米波阵列天线

5G标准工具包

- 编码输入
- 功率密度计算
- 累计分配功能
- 完全参数化



最大允许接触：功率密度




5G Wizard


Project/Design

Projects: 5G_28GHz_AntennaModule_2020R1

Design: 4x1_array1

Solution/Setup

Setup: Setup1:LastAdaptive

Frequency: 28.0GHz

Beam ID Codebook

Codebook (*.csv): C:\Users\asligar\Documents\Applications\PC\ Browse ?

☐ Include Beam Pair ?

☒ Update Beam ID Codebook (Applies Immediately) ?

Power Density Settings

☒ Do Power Density Calculation

Beam ID Variable Select: beamID ?

Power Density Surface: 5mm_Surface ?

Step Size (mm): 2 ?

Averaging Area (cm²): 4 ?

5G Wizard: Automated PD Extraction

5G天线阵性能建模

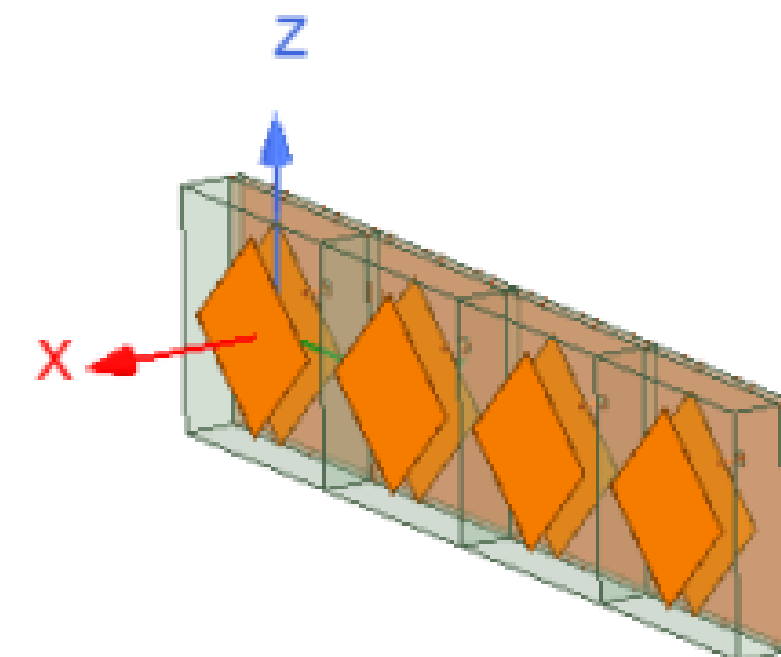
Antenna Beam Steering

- Antenna beam formed *using look-up table: **Code Book***
- Look-up table imported into HFSS
 - User can control beam by selecting corresponding beam ID

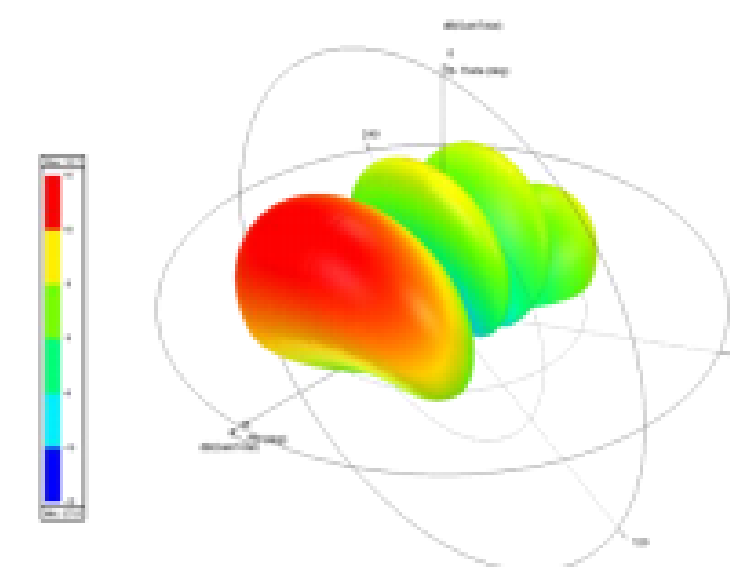
Beam ID	Port 1	Port 2	Port 3	Port 4
1	1W @ 0°	1W @ -145°	1W @ -290°	1W @ -435°
2	1W @ 0°	1W @ -84°	1W @ -168°	1W @ -252°
3	1W @ 0°	1W @ 0°	1W @ 0°	1W @ 0°
4	1W @ 0°	1W @ 84°	1W @ 168°	1W @ 252°
5	1W @ 0°	1W @ 145°	1W @ 290°	1W @ 435°

HFSS supports Code Book definition for port excitations

Automated
look-up table
application to mm-
wave array
using scripting



Beam pattern selected by Beam ID post processing variable



分布式直接求解器内存改进

- Multi-package module 264 ports

	Time	Memory
Old	48:03	181 GB
New	20:56	143 GB (20% savings)

- Multi-package module 764 ports

	Time	Memory
Old	5:36:11	595 GB
New	1:42:45	498 GB (16% savings)

IC Package model, 34.5M matrix unknowns

2020 R1

Adaptive Meshing

Elapsed time: 04:12:25, total memory: **552.4 GB**

Frequency Sweep

Elapsed time: **07:32:11**

2020 R2

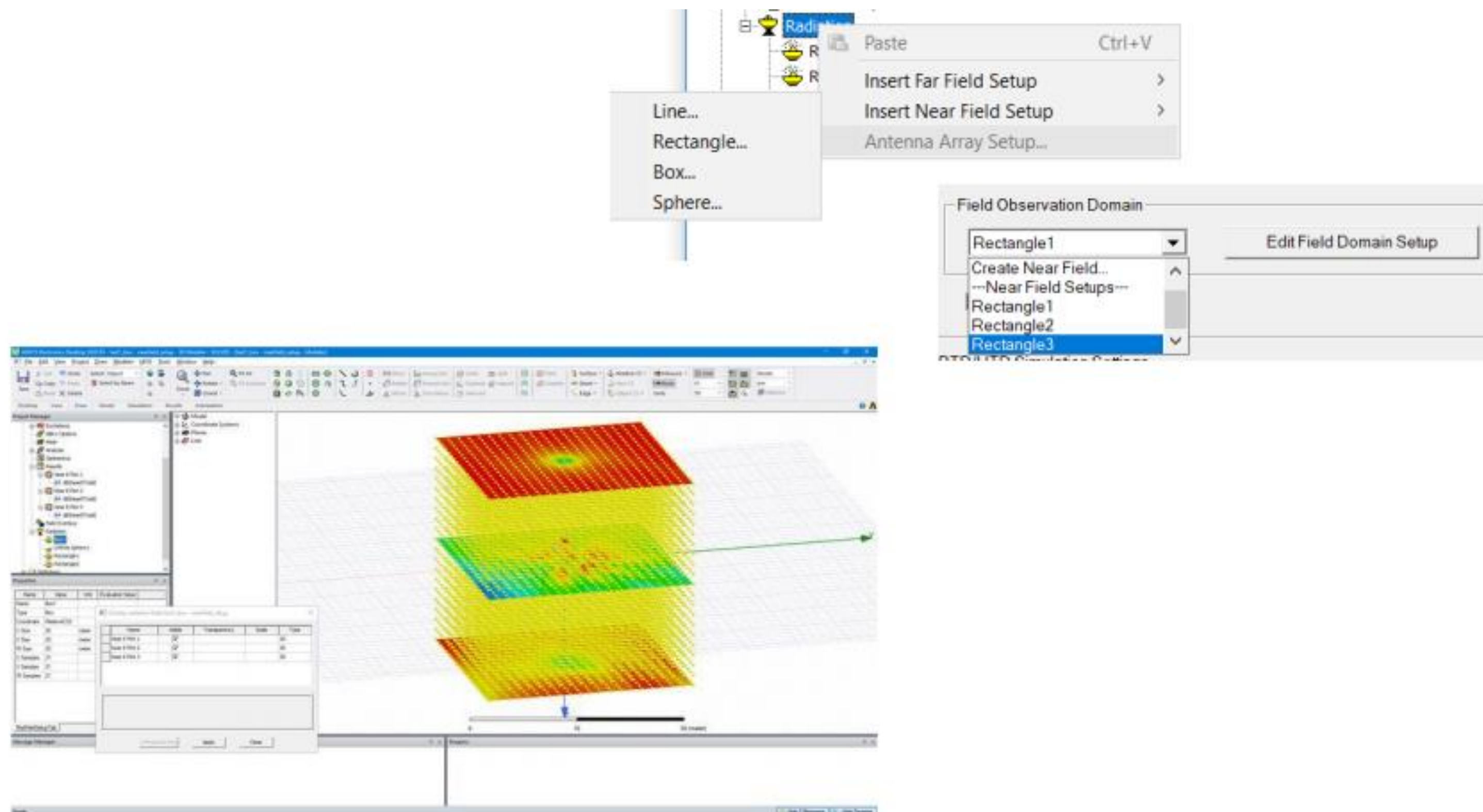
Adaptive Meshing

Elapsed time: 02:48:27, total memory: **421.6 GB** (24% savings)

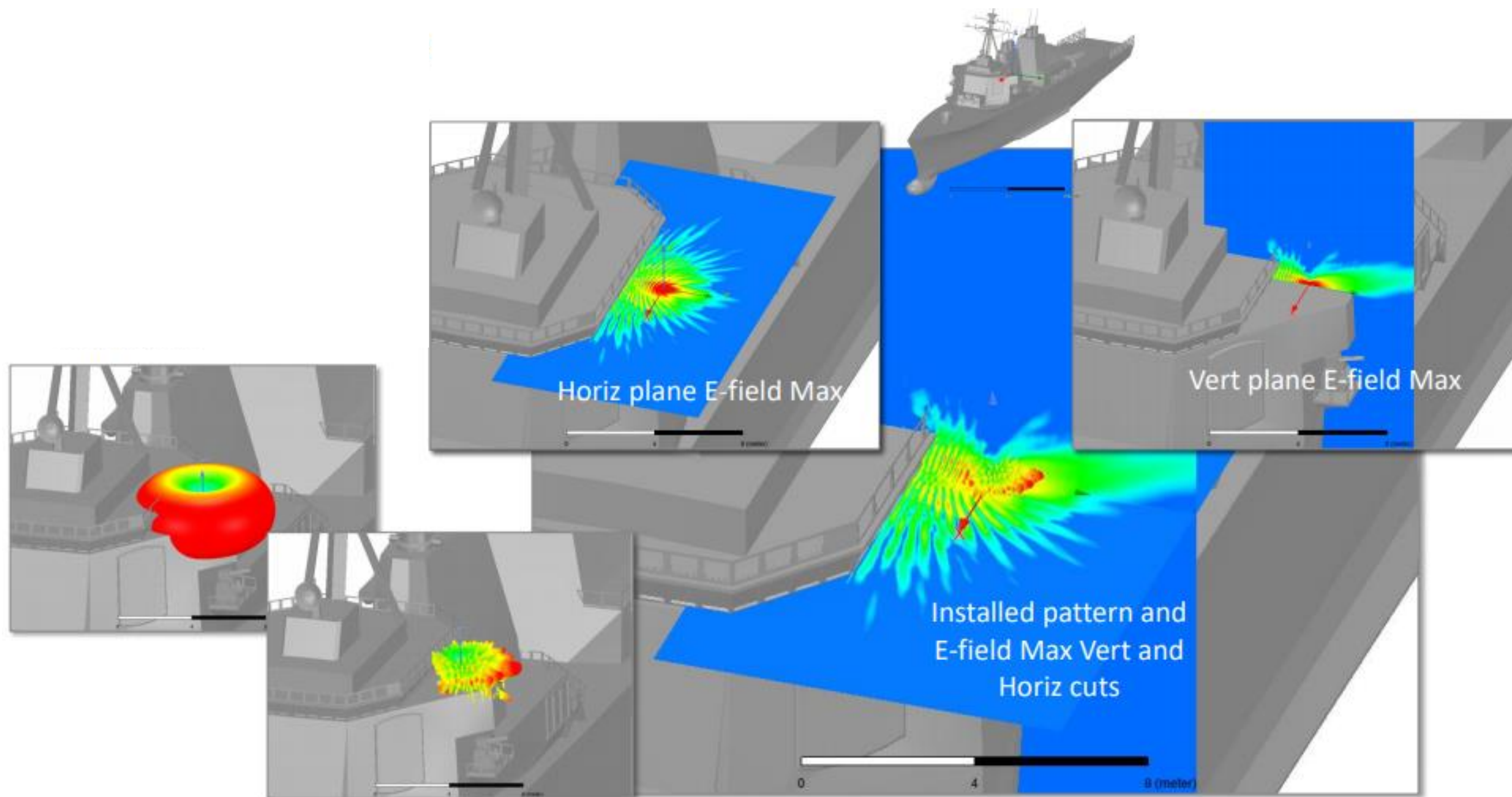
Frequency Sweep (More Freq points in II)

Elapsed time: **05:53:59 (22% faster)**

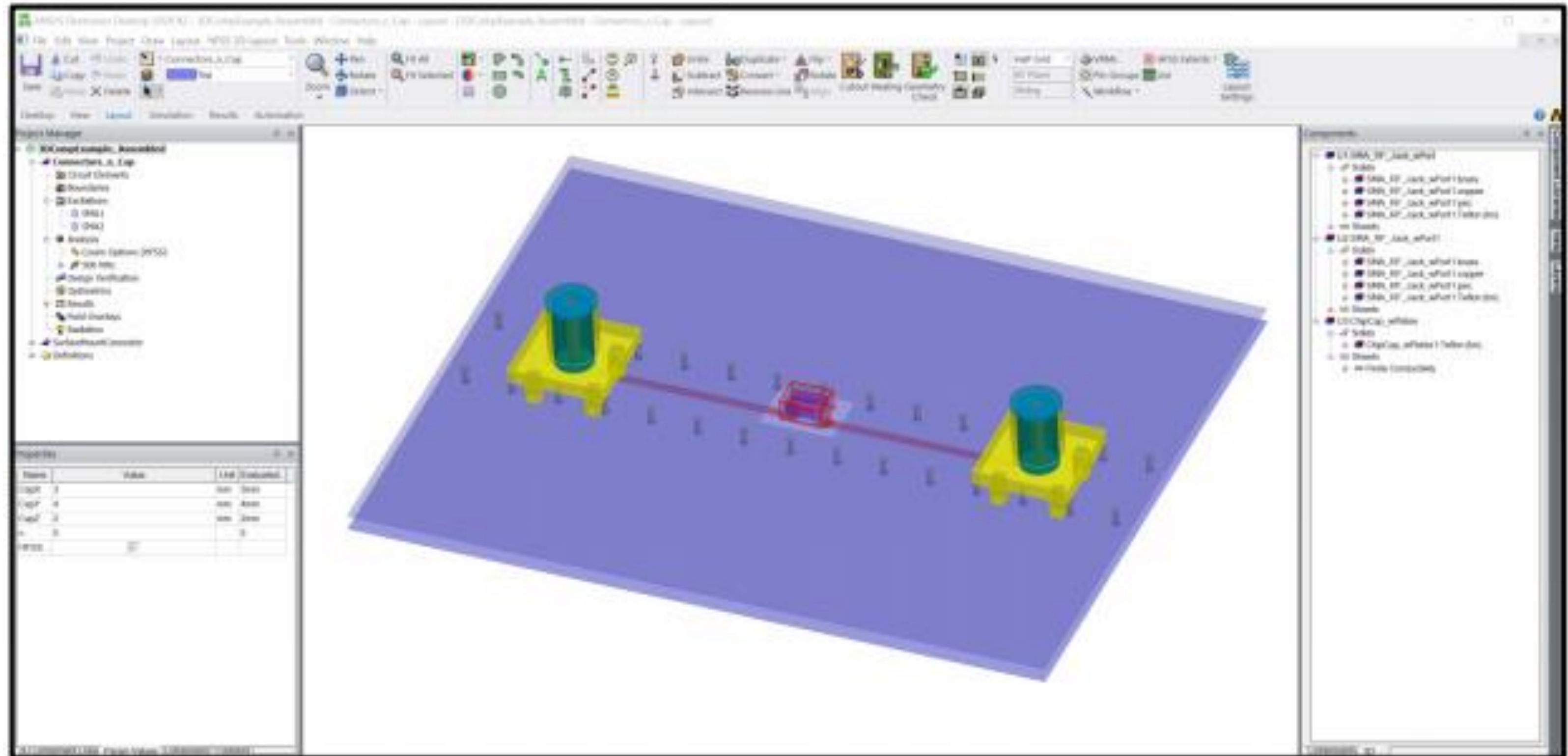
SBR+近场分析



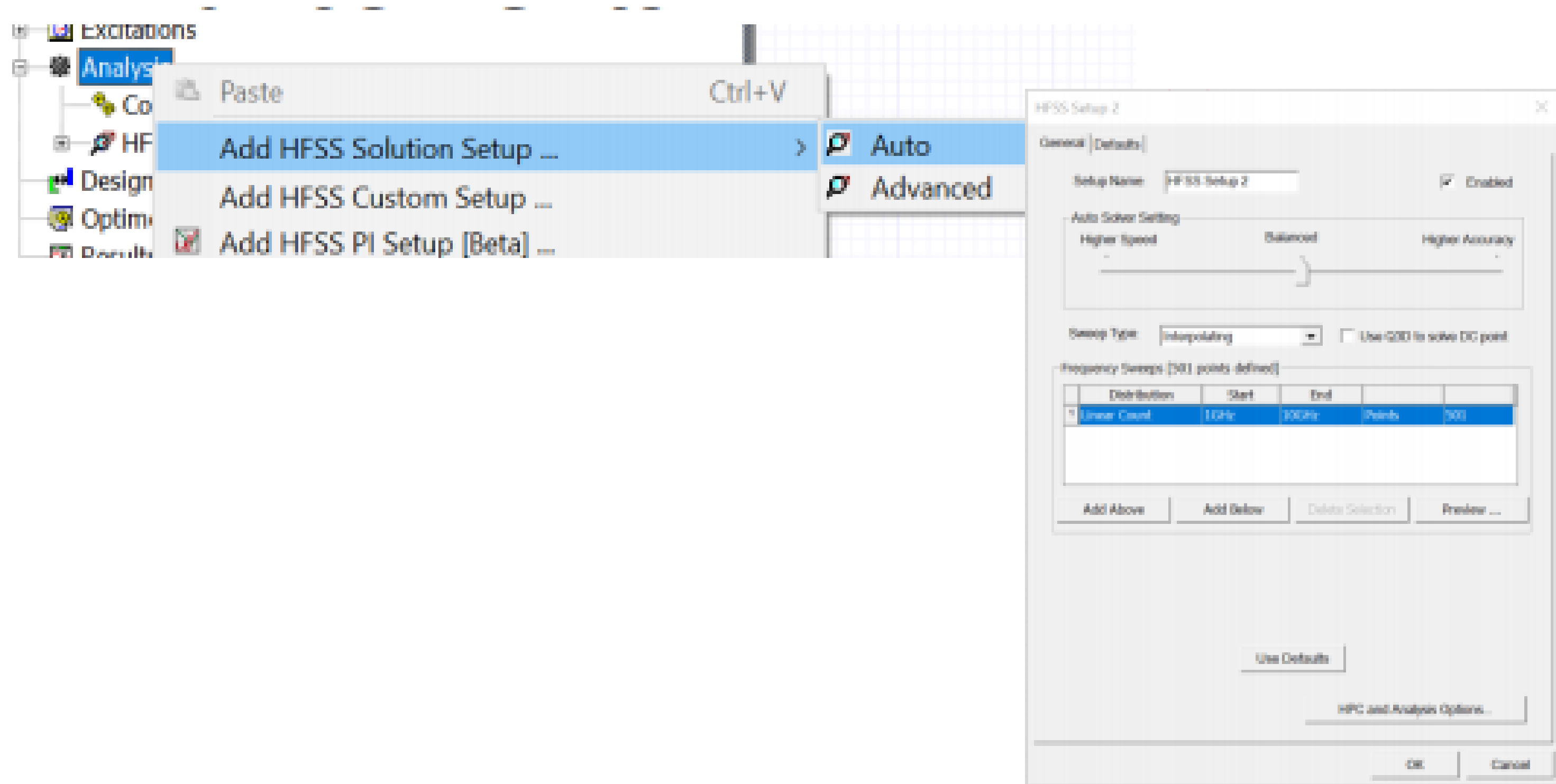
SBR+近场分析



HFSS 3D Layout支持3D组件



HFSS 3D Layout也支持Auto Setup

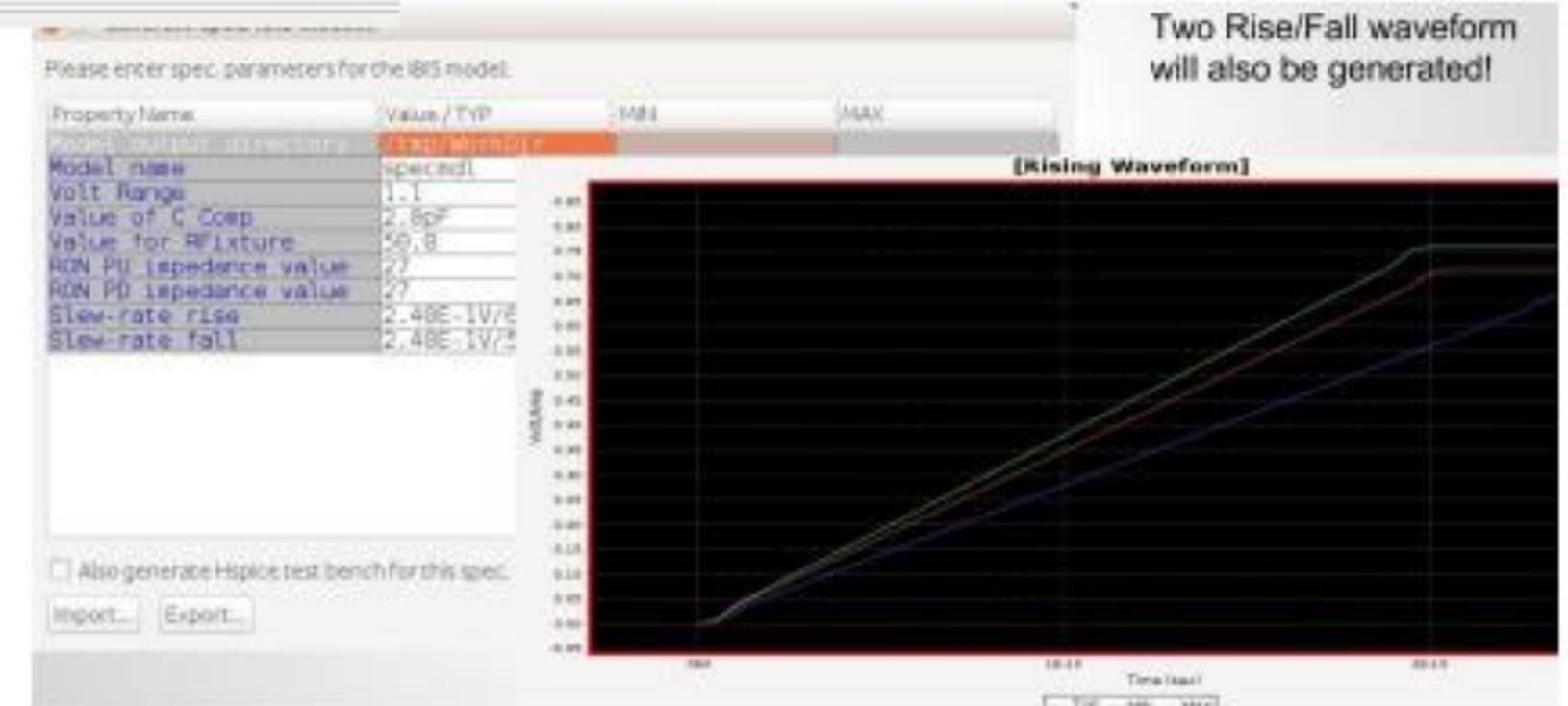
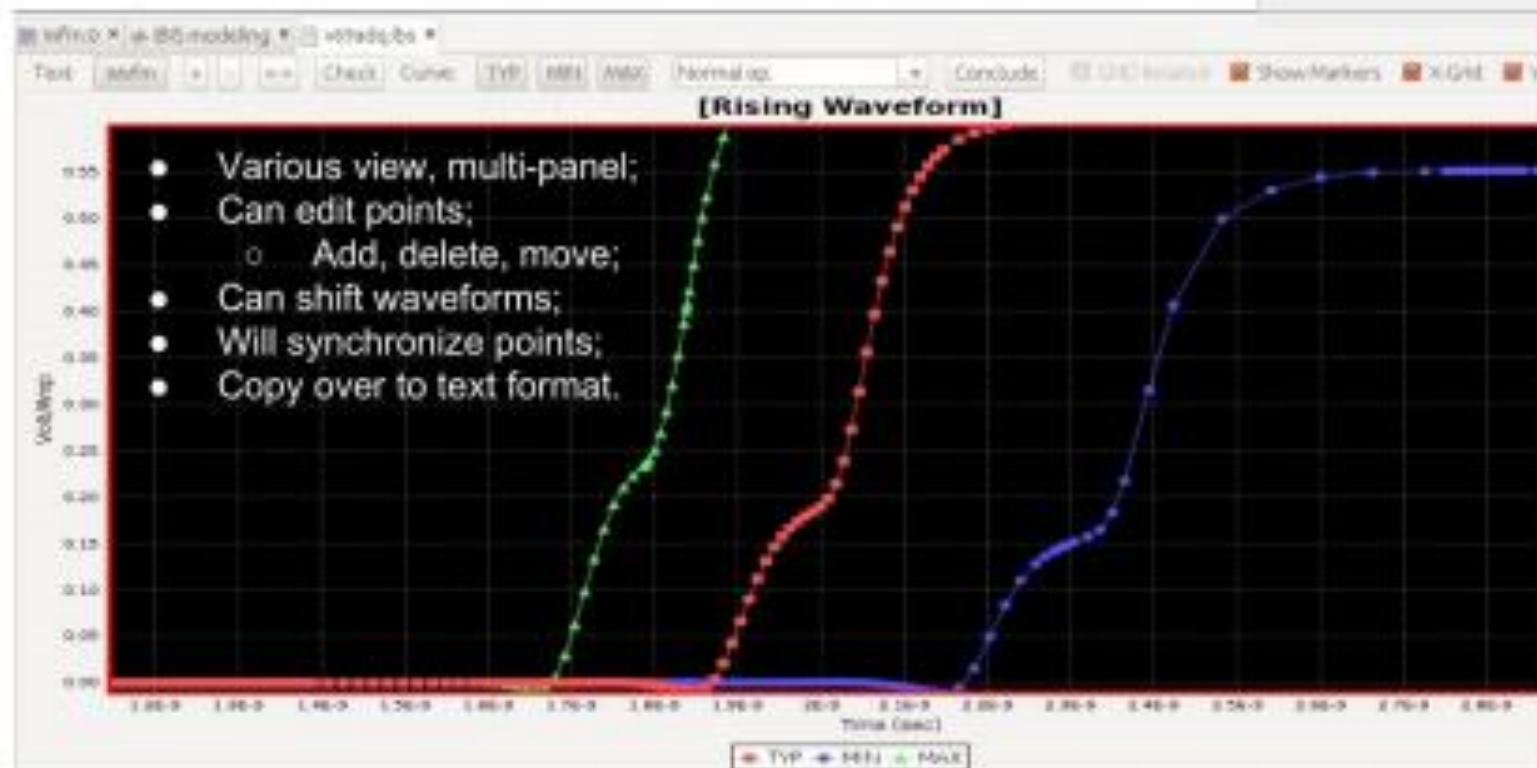
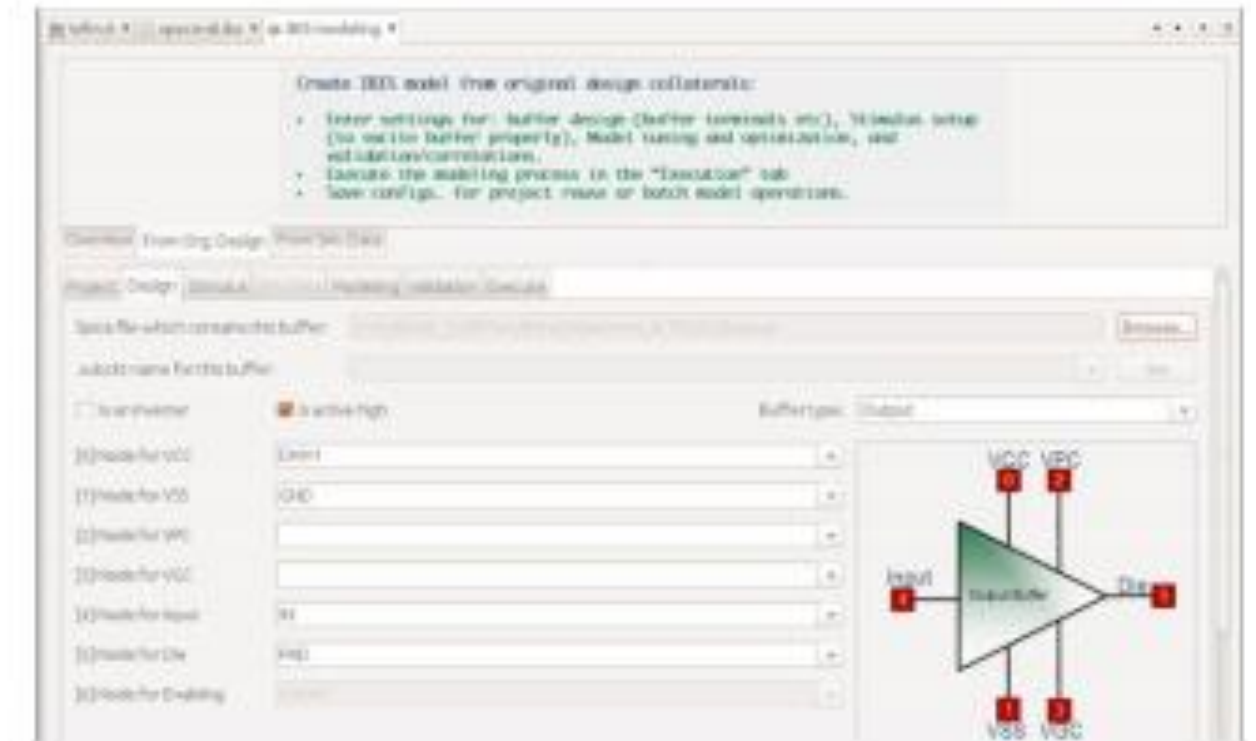
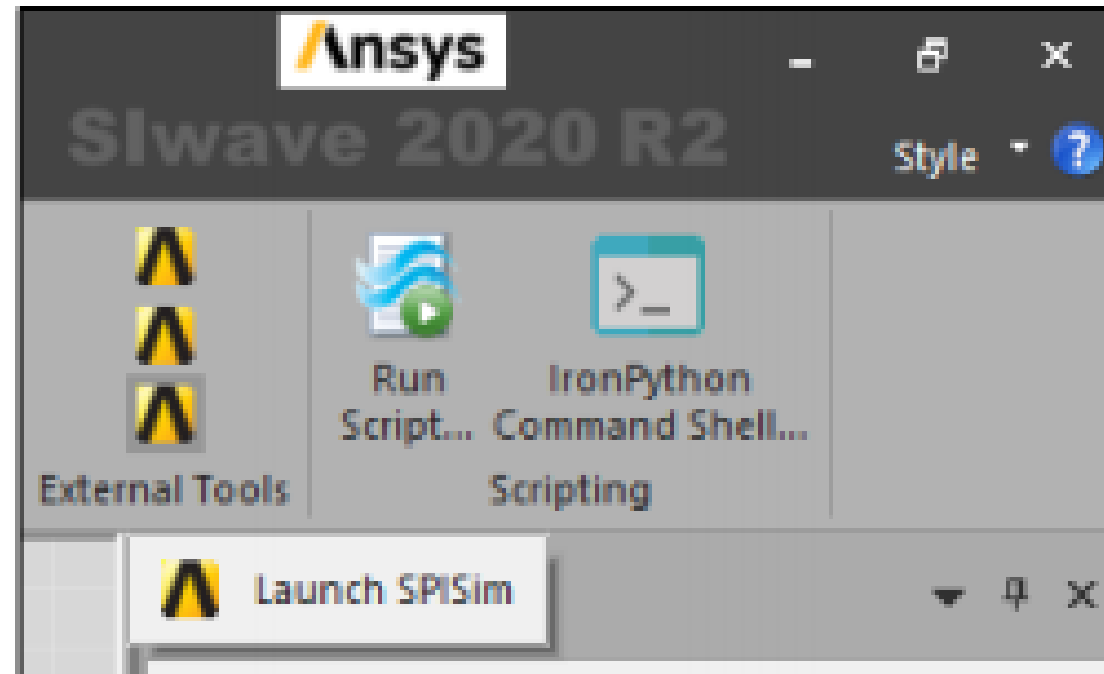


Signal & Power Integrity

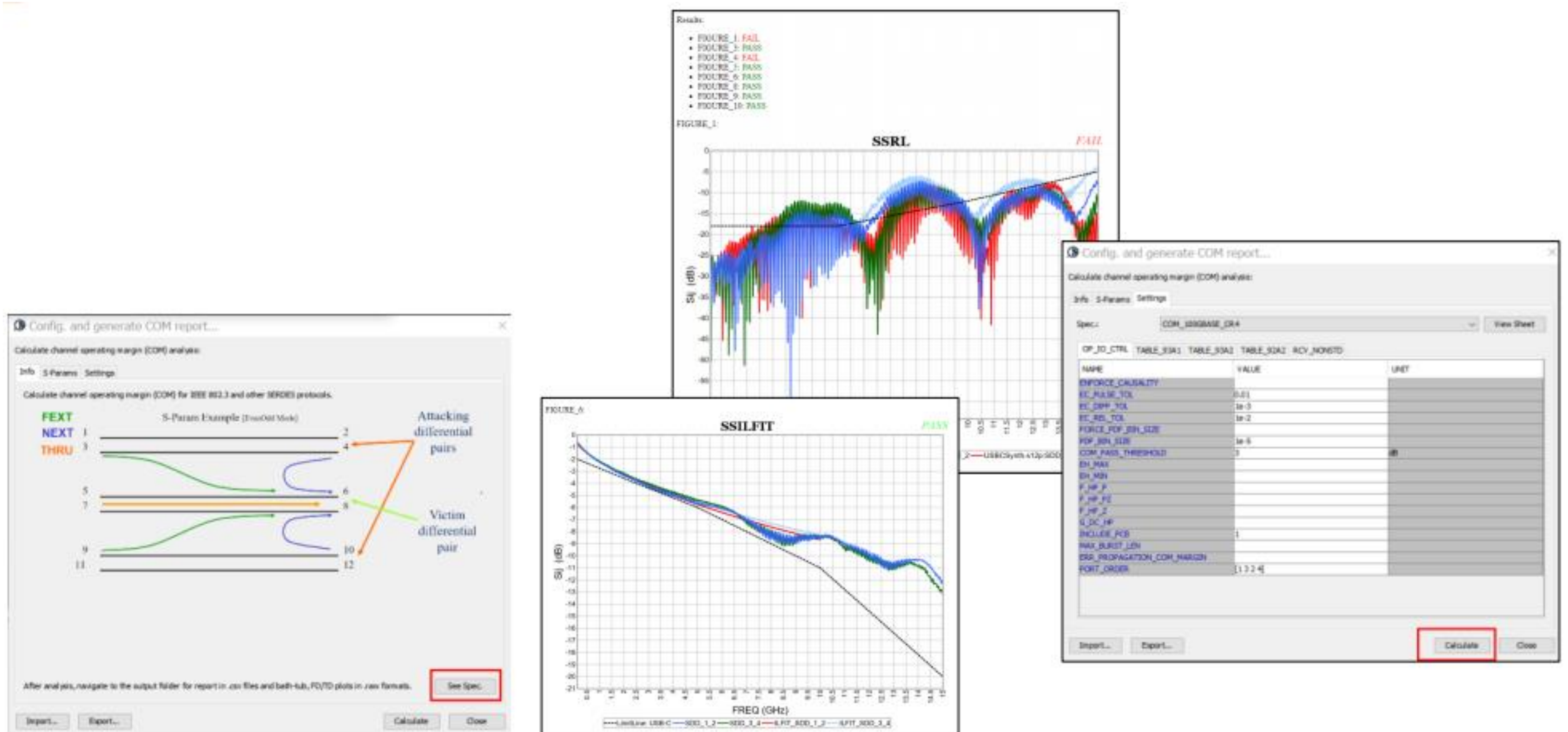
关键更新点

- SPISim – IBIS和802.3ac (COM)/USB-C通道符合性 (new)
- SIwave
 - 对Z0 Scanner & SNA后处理的增强
 - CPA Smart Pin Grouping & Settings增强 (new)
 - 求解器改进
- HFSS 3D Layout
 - 3D Layout支持3D元件
 - 对3D IC封装工作流程的 “IC” 模式求解器设置[Beta] (new)
 - 3D Layout支持Auto Solution Setup
- Q3D Extractor
 - 绘制求解区域外的电场
- Circuit
 - 功率电子的收敛改进

SPISim技术-IBIS Modeling

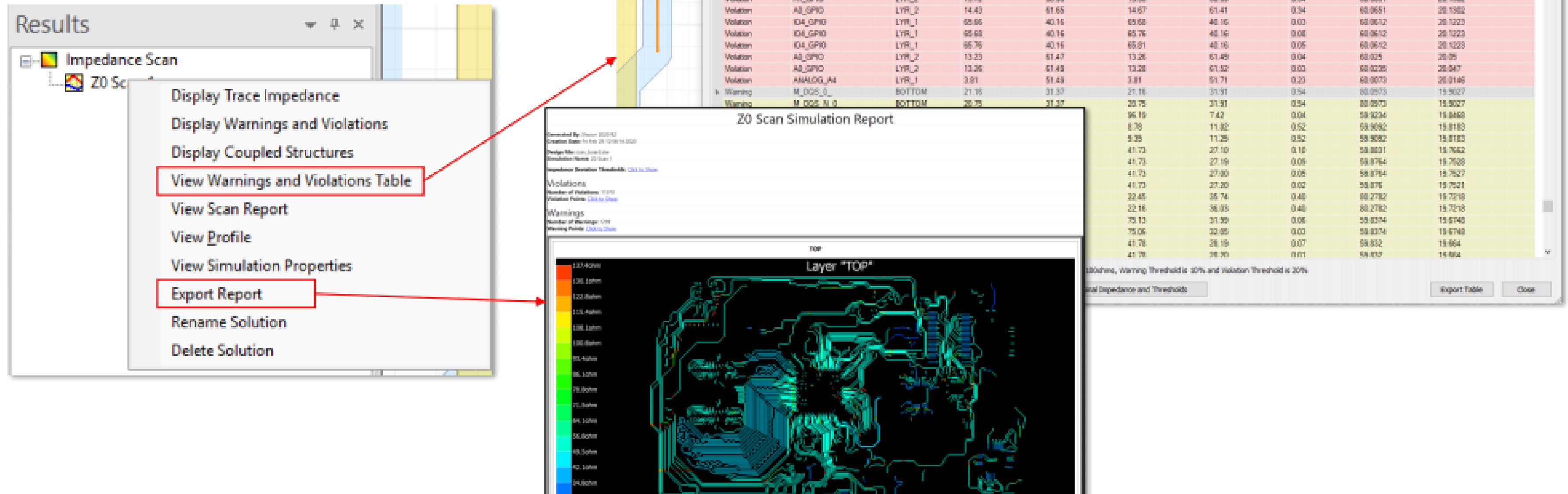


SPI Sim技术-COM和USB通道符合度测试



SIwave - Impedance Scan后处理增强

- Interactive trace impedance navigation
- Full-design trace impedance summary HTML report export



Results

- Impedance Scan
- Z0 Scan
 - Display Trace Impedance
 - Display Warnings and Violations
 - Display Coupled Structures
 - View Warnings and Violations Table**
 - View Scan Report
 - View Profile
 - View Simulation Properties
 - Export Report**
 - Rename Solution
 - Delete Solution

Z0 Scan Simulation Report

Generated By: SIwave 2024.12
 Creation Date: Fri Feb 28 10:08:10 2020
 Design File: ...
 Simulation Name: Z0 Scan 1
 Impedance Deviation Threshold: 30% (Show)

Violations
 Number of Violations: 10/10
 Violation Points: (Show)

Warnings
 Number of Warnings: 1/1
 Warning Points: (Show)

Layer	Start Point X (mm)	Start Point Y (mm)	End Point X (mm)	End Point Y (mm)	Length (mm)	Impedance (ohms)	Impedance Deviation (%)
LYR_1	59.83	22.68	59.88	22.68	0.05	60.1111	20.2222
BOTTOM	21.56	33.50	22.00	33.50	0.43	79.832	20.168
BOTTOM	21.56	33.54	22.00	33.54	0.43	79.832	20.168
BOTTOM	22.00	33.50	22.10	33.50	0.11	79.832	20.168
BOTTOM	22.00	33.54	22.10	33.54	0.11	79.832	20.168
LYR_2	51.89	31.67	52.17	31.67	0.28	60.0896	20.1612
LYR_2	51.89	30.63	52.17	30.63	0.28	60.0896	20.1612
LYR_2	59.82	42.60	59.82	42.70	0.10	60.0779	20.1559
LYR_2	59.82	42.70	59.82	42.77	0.08	60.0779	20.1559
LYR_2	13.72	60.99	13.96	60.99	0.24	60.0651	20.1362
LYR_2	14.43	61.65	14.67	61.65	0.24	60.0651	20.1362
LYR_1	65.66	40.16	65.66	40.16	0.00	60.0612	20.1223
LYR_1	65.66	40.16	65.76	40.16	0.08	60.0612	20.1223
LYR_1	65.76	40.16	65.81	40.16	0.05	60.0612	20.1223
LYR_2	13.23	61.47	13.26	61.48	0.04	60.035	20.05
LYR_2	13.26	61.48	13.26	61.52	0.03	60.0325	20.047
LYR_1	3.81	51.49	3.81	51.71	0.23	60.0073	20.0146
BOTTOM	21.16	31.37	21.16	31.91	0.54	60.0073	19.9027
BOTTOM	20.75	31.37	20.75	31.91	0.54	60.0073	19.9027
						59.9234	19.8469
						59.9082	19.8183
						59.9082	19.8183
						59.8831	19.7662
						59.8764	19.7528
						59.8764	19.7527
						59.876	19.7521
						60.2762	19.7218
						59.8374	19.6748
						59.8374	19.6748
						59.832	19.664
						59.832	19.664

3D Model: Layer "TOP" showing impedance distribution with a color scale from 120.4ohms (red) to 34.0ohms (blue).

Legend: 120.4ohms, 120.1ohms, 122.0ohms, 119.4ohms, 118.1ohms, 116.0ohms, 114.0ohms, 112.0ohms, 110.0ohms, 108.0ohms, 106.0ohms, 104.0ohms, 102.0ohms, 100.0ohms, 98.0ohms, 96.0ohms, 94.0ohms, 92.0ohms, 90.0ohms, 88.0ohms, 86.0ohms, 84.0ohms, 82.0ohms, 80.0ohms, 78.0ohms, 76.0ohms, 74.0ohms, 72.0ohms, 70.0ohms, 68.0ohms, 66.0ohms, 64.0ohms, 62.0ohms, 60.0ohms, 58.0ohms, 56.0ohms, 54.0ohms, 52.0ohms, 50.0ohms, 48.0ohms, 46.0ohms, 44.0ohms, 42.0ohms, 40.0ohms, 38.0ohms, 36.0ohms, 34.0ohms.

Warning Threshold is 10% and Violation Threshold is 30%.

Export Table Close

SIwave – 网络时延的计算输出

Signal Net Analyzer



Signal Net Analyzer (SNA) Net Delay Report

Generated By: SIwave 2020 R2
Creation Date: Fri Feb 28 13:08:00 2020

Design File: scan_board.siw

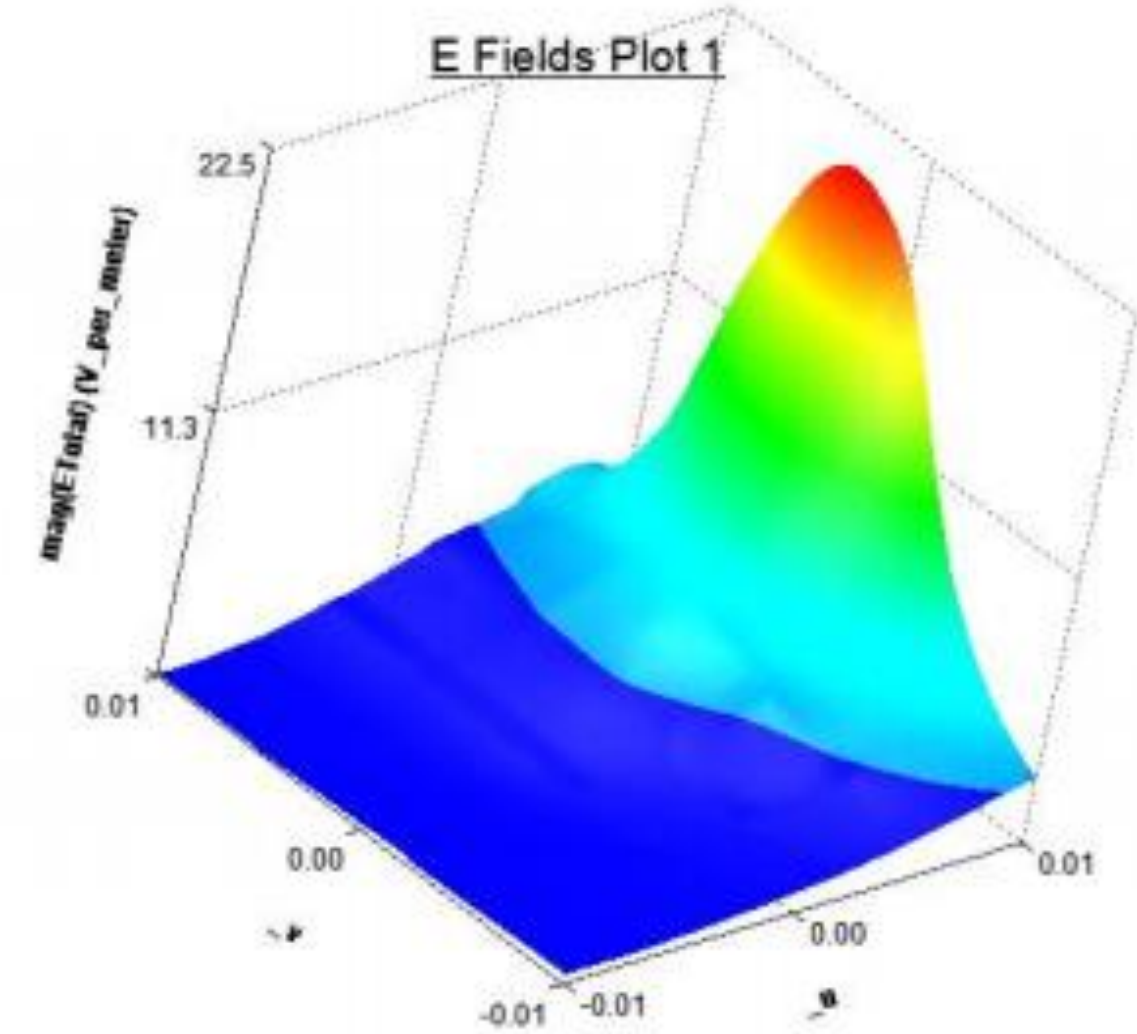
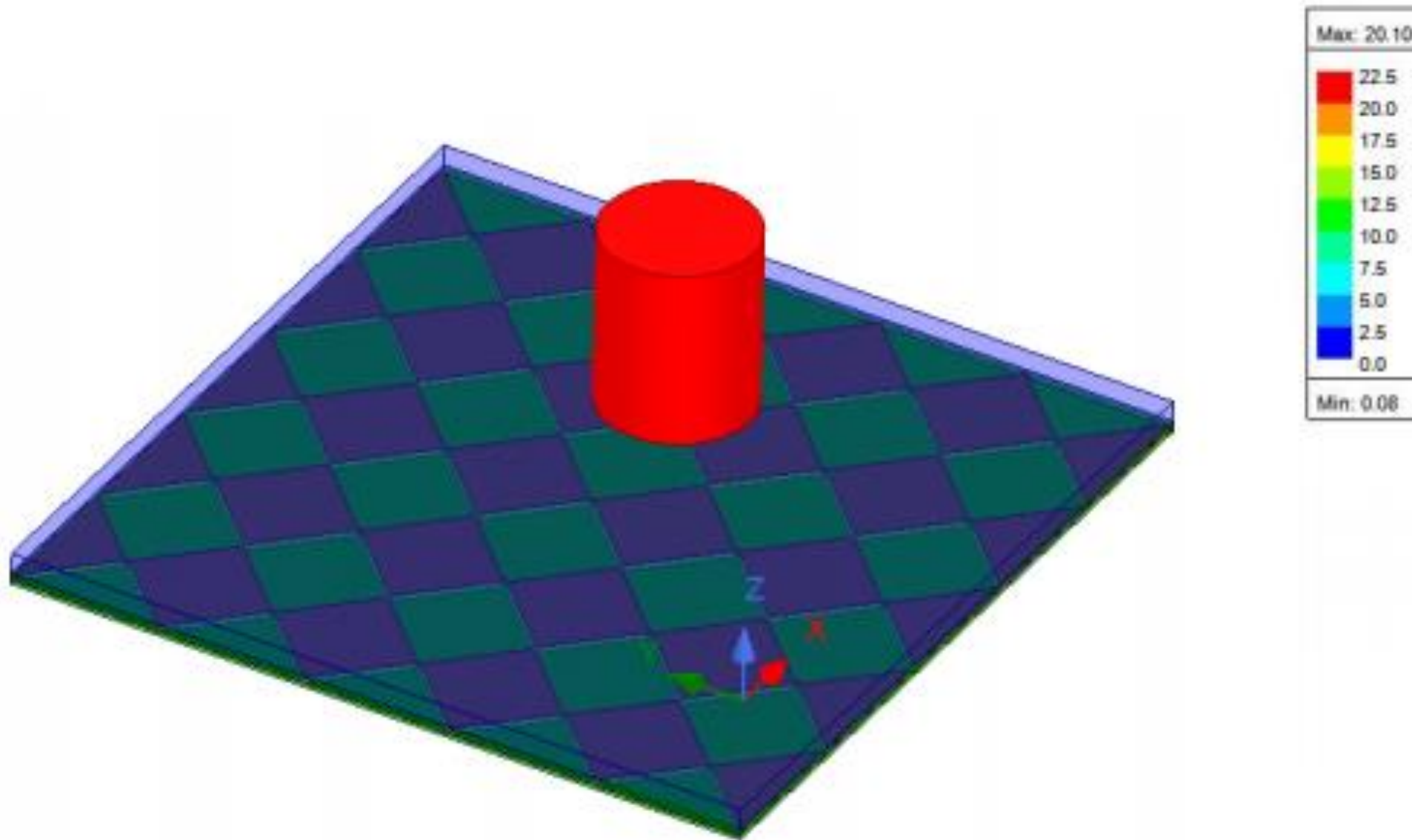
Table sorted by: Differential Delay Mismatch
(Switch to sort by Net)
(Switch to sort by Length)
(Switch to sort by Delay)

Table Filter: * All * Single-Ended * Differential * Extended * Extended-Differential

Net	Start Pin	End Pin	Length (mm)	Differential Pair Length Mismatch (mm)	Delay (ps)	Differential Pair Delay Mismatch (ps)
PCIE0_TX0_P_C (Differential Net: DP_PCIE0_TX0 (PCIE0_TX0_P_C and PCIE0_TX0_P))	C3A4:1	U2A5:AD3	62.260	58.731	370.895	355.017
PCIE0_TX0_P (Differential Net: DP_PCIE0_TX0 (PCIE0_TX0_P_C and PCIE0_TX0_P))	C3A4:2	U2L1:33	3.529	-58.731	15.878	-355.017
RMII_S0_TDP (Differential Net: DP_RMII_S0_TD (RMII_S0_TDP and RMII_S0_TDN)) - Path 1	R1M10:2	J4B1:11	36.163	-1.465	216.707	-8.860
RMII_S0_TDN (Differential Net: DP_RMII_S0_TD (RMII_S0_TDP and RMII_S0_TDN)) - Path 1	R1M9:2	J4B1:10	37.628	1.465	225.567	8.860
RMII_S0_TDP (Differential Net: DP_RMII_S0_TD (RMII_S0_TDP and RMII_S0_TDN)) - Path 2	R1M10:2	U4B1:17	8.234	2.253	44.264	8.819
RMII_S0_TDN (Differential Net: DP_RMII_S0_TD (RMII_S0_TDP and RMII_S0_TDN)) - Path 2	R1M9:2	U4B1:16	5.981	-2.253	35.445	-8.819
USBH2_DP_CH (Differential Net: DP_USBH2_D_CH (USBH2_DP_CH and USBH2_DN_CH)) - Path 0	L3M1:0:2	J3B2:3	12.588	0.307	71.640	1.881
USBH2_DN_CH (Differential Net: DP_USBH2_D_CH (USBH2_DP_CH and USBH2_DN_CH)) - Path 0	L3M1:1:3	J3B2:2	12.281	-0.307	69.759	-1.881
M_DQS_N_0_ (Differential Net: DP_M_DQS0 (M_DQS_N_0_ and M_DQS_0_))	U2A5:AH7	U1B5:D3	36.396	0.301	214.142	1.832
M_DQS_0_ (Differential Net: DP_M_DQS0 (M_DQS_N_0_ and M_DQS_0_))	U2A5:AK7	U1B5:C3	36.095	-0.301	212.310	-1.832
USBH2_DP_CH (Differential Net: DP_USBH2_D_CH (USBH2_DP_CH and USBH2_DN_CH)) - Path 2	L3M1:0:2	U2B3:B1	4.636	0.285	22.734	1.738
USBH2_DN_CH (Differential Net: DP_USBH2_D_CH (USBH2_DP_CH and USBH2_DN_CH)) - Path 2	U2B3:A2	L3M1:1:3	4.350	-0.285	20.996	-1.738
USBH0_DP_CH (Differential Net: DP_USBH0_D_CH (USBH0_DP_CH and USBH0_DN_CH)) - Path 2	U2B2:B1	L3M2:1:3	4.559	0.264	22.272	1.617
USBH0_DN_CH (Differential Net: DP_USBH0_D_CH (USBH0_DP_CH and USBH0_DN_CH)) - Path 2	U2B2:A2	L3M2:0:2	4.295	-0.264	20.655	-1.617
USBH0_DP_CH (Differential Net: DP_USBH0_D_CH (USBH0_DP_CH and USBH0_DN_CH)) - Path 0	L3M2:1:3	J2B3:3	10.556	0.169	59.165	1.043
USBH0_DN_CH (Differential Net: DP_USBH0_D_CH (USBH0_DP_CH and USBH0_DN_CH)) - Path 0	L3M2:0:2	J2B3:2	10.387	-0.169	58.122	-1.043
M_CLK_N_0_ (Differential Net: DP_M_CLK0 (M_CLK_N_0_ and M_CLK_0_)) - Path 1	U2A5:AL30	U1A1:G7	78.816	-0.097	484.245	-0.924
M_CLK_0_ (Differential Net: DP_M_CLK0 (M_CLK_N_0_ and M_CLK_0_)) - Path 1	U2A5:AJ30	U1A1:F7	78.913	0.097	485.169	0.924
M_CLK_N_0_ (Differential Net: DP_M_CLK0 (M_CLK_N_0_ and M_CLK_0_)) - Path 0	U2A5:AL30	R4L10:1	85.041	-0.383	531.872	-0.833

Q3D后处理

- Electric field visualization for capacitance solver
- Calculations on line, rectangle, box, and sphere



E-field above touch panel

ECAD导入导出版本支持

- Cadence SPB Tools (direct import of *.mcm, *.brd & *.sip files into HFSS 3D Layout only)
 - Allegro, APD and SiP Digital/RF 16.0, 16.1, 16.2, 16.3, 16.5, 16.6 and 17.2
- Zuken Tools (direct import of *.pcf files)
 - Zuken CR5000 10 and later
 - Zuken CR8000 2013 and later
- Mentor (direct import of *.asc files)
 - PADS PowerPCB v5.2a, v2005 and v2007
- ODB++ Layouts
 - Altium Designer R10 and later
 - Mentor Expedition EE7.9.1 and later
 - Mentor PADS 9.4 and later (v7 and v8 ODB++)
 - Zuken Cadstar 12.1 and later
- IPC2581 Layouts
 - Pulsonix R8.5 build 5905 and later

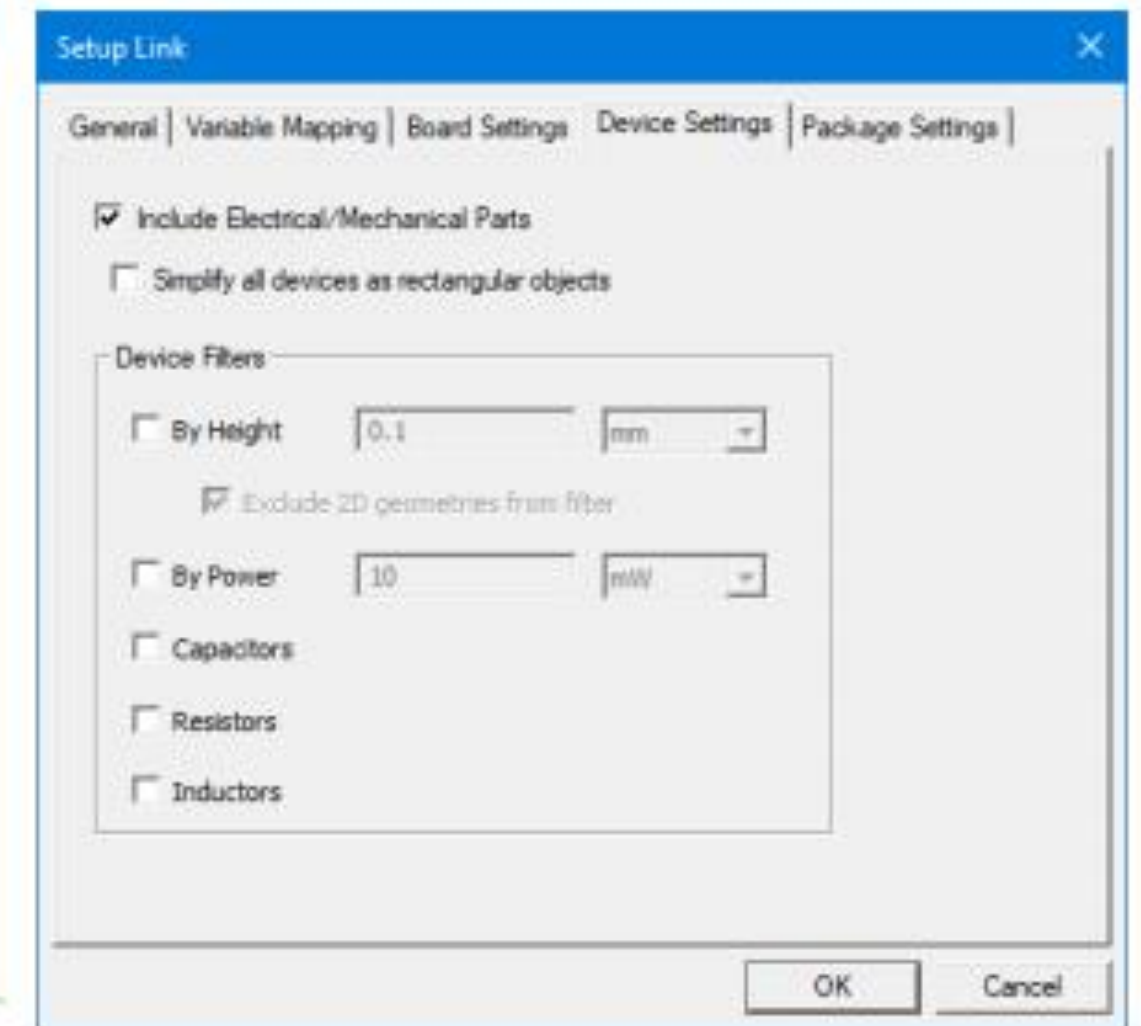
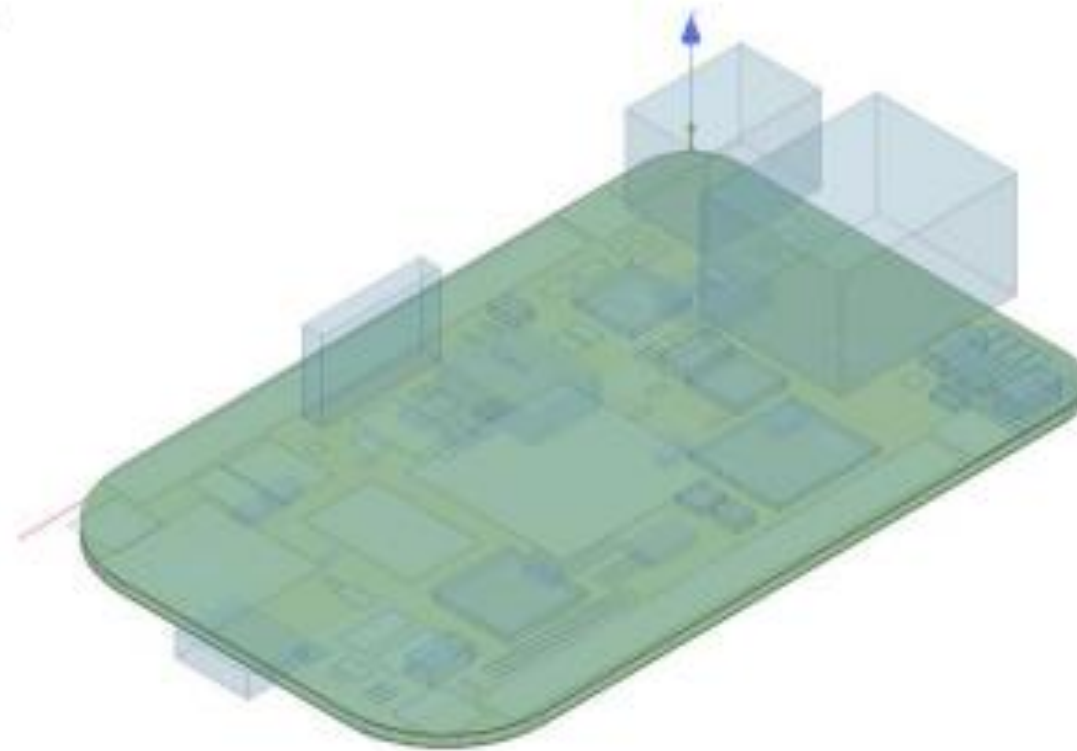
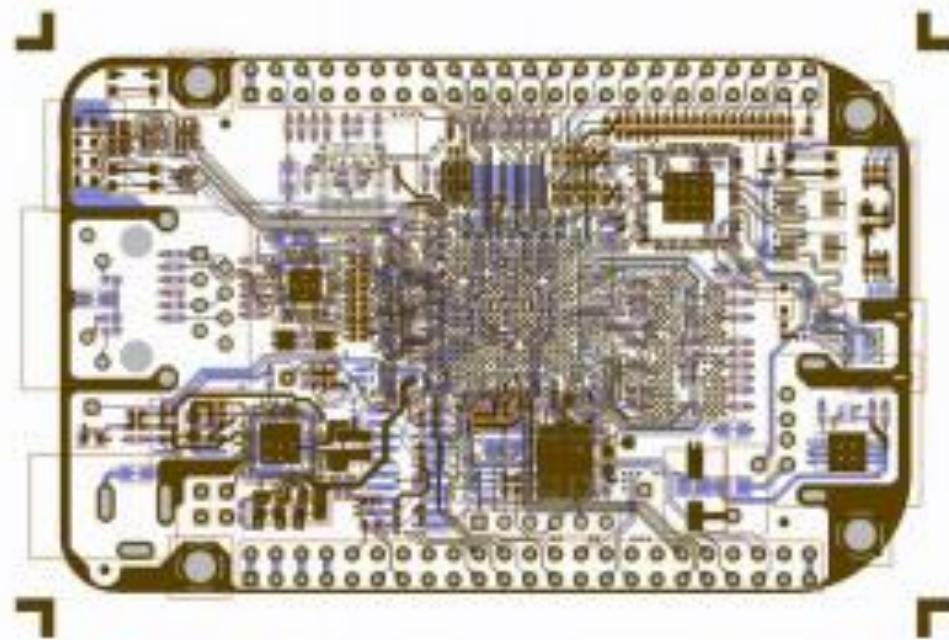
Electronics Thermal Integrity

关键更新点

- PCB 3D元件 – Component data & Flip-chip BGA
- 网格改进 – Concurrent meshing & Import for AEDT
- 动态热管理
- 自动化工具 – New PCB & Solar Loading Toolkits
- MCAD Faceting slider bar
- ECXML Import in AEDT
- 机械热设计 [Beta] – EM Loss & Icepak link enhancements

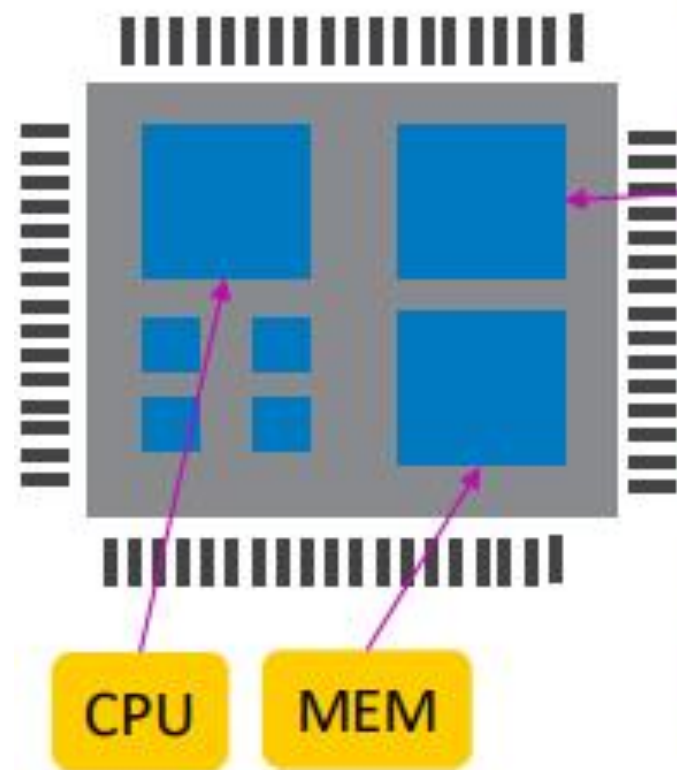
ECAD: 采用PCB元件形式导入IDF数据和封装数据

- IDF data is part of PCB Component
 - Import all device data through 3D Layout using Setup Link
 - Support Blocks and Source BCs
 - Device geometries part of PCB
 - Alternative to separate IDF import
- Support ODB++ and IPC-2581



增强瞬态模型 – 动态热管理

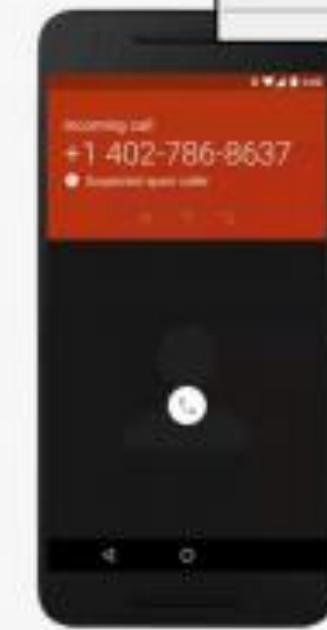
- Power throttling capability based on local temperatures
- Temperature-dependent profiles controlled by scripts
- Python scripting supported
 - New 'DTM' source BC specification
 - Simulation control tab to pick user-defined script



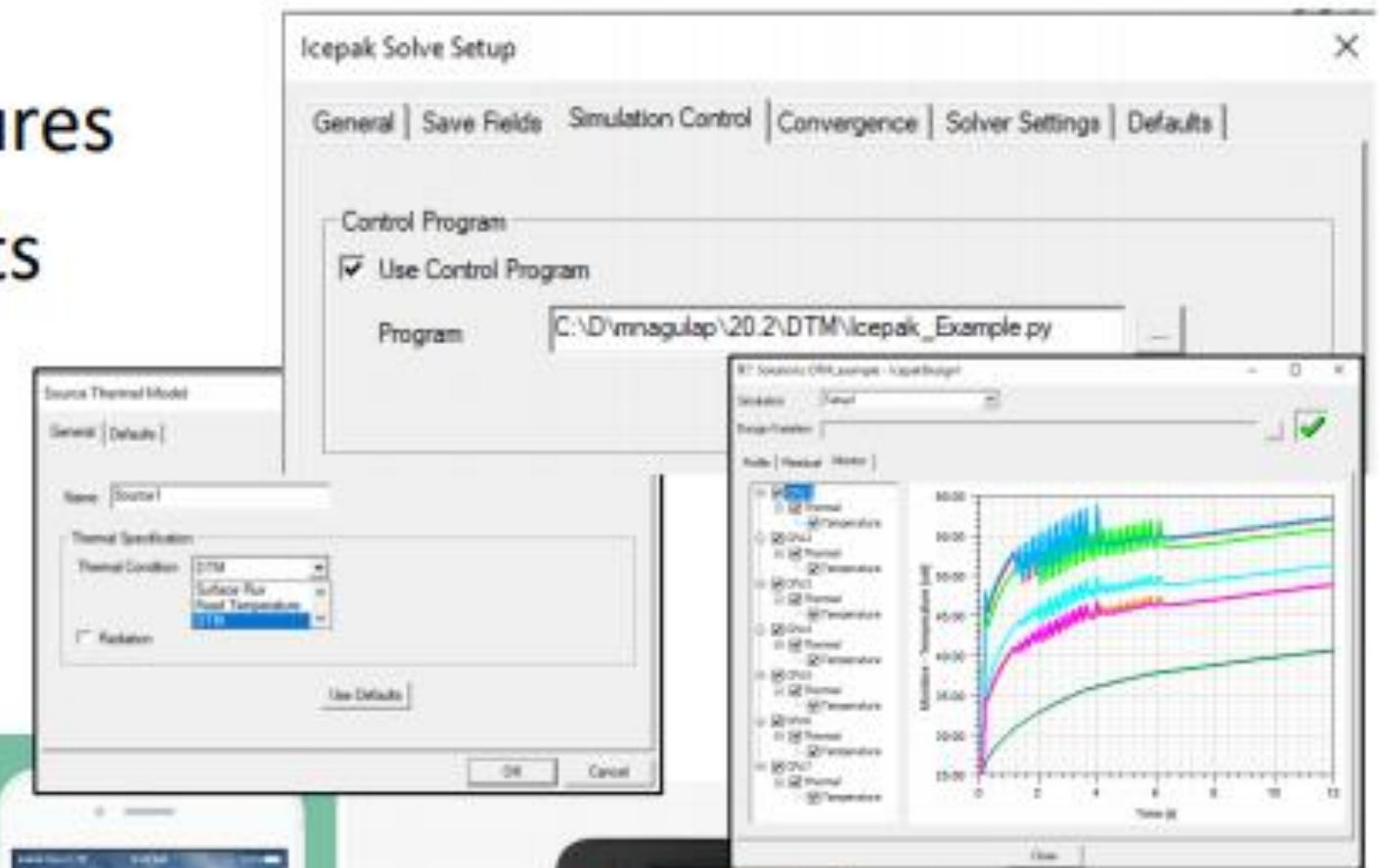
Camera



Browsing + GPS

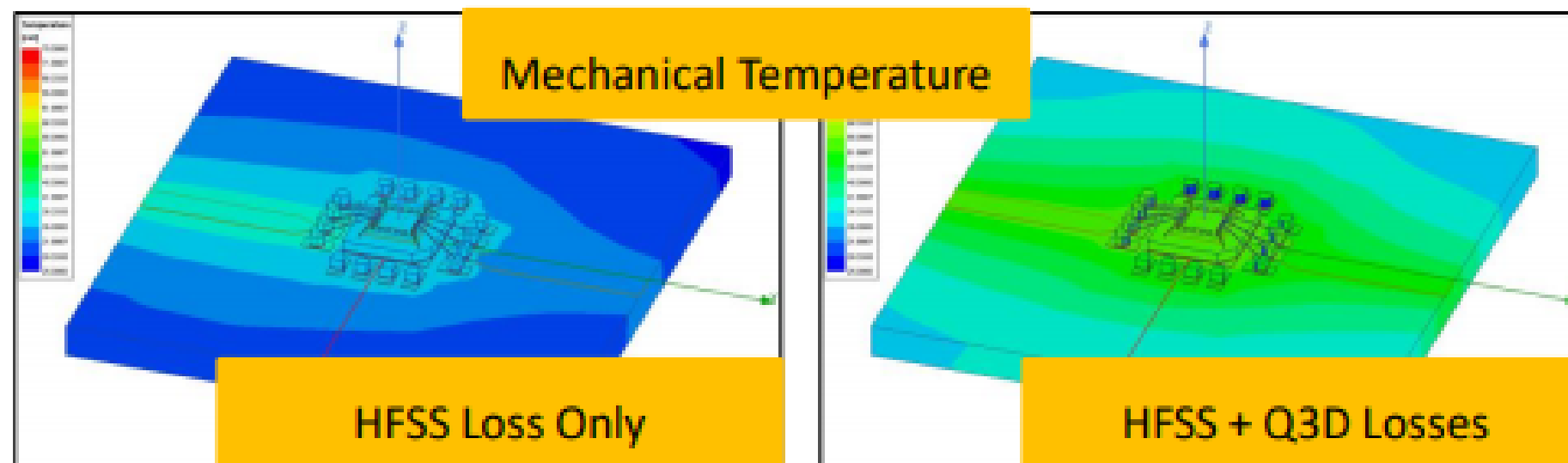
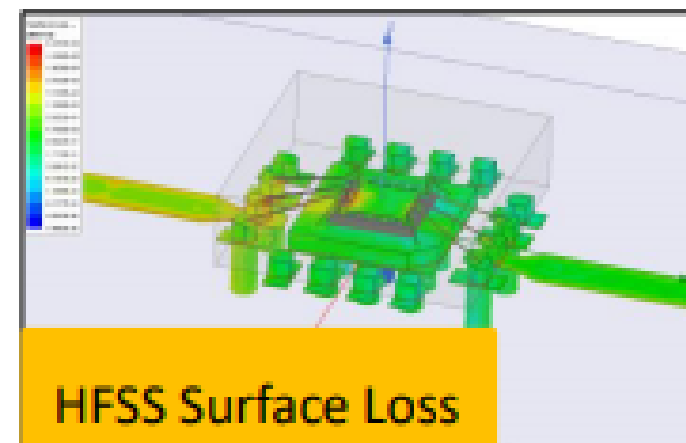
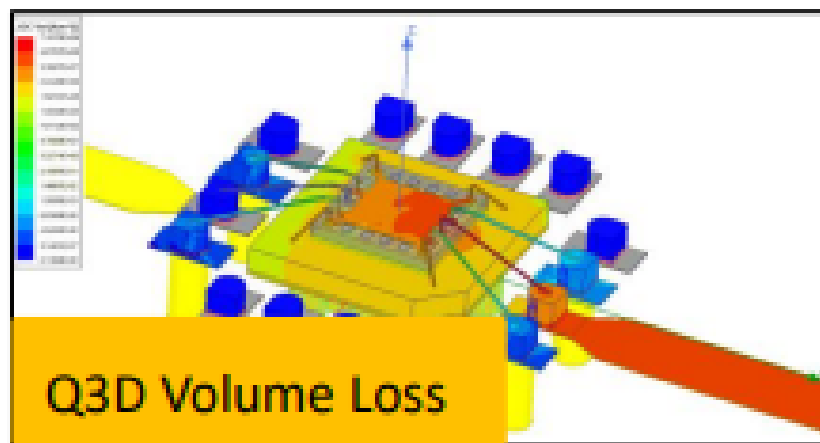


Call

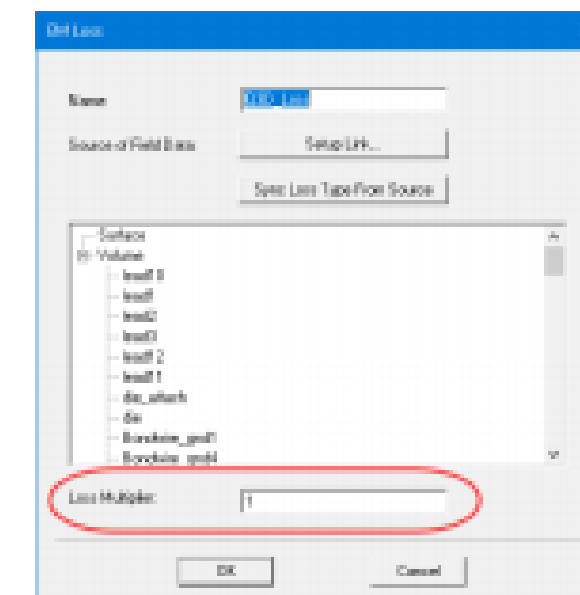


AEDT 机械-电磁损耗增强

- Ability to combine losses on identical objects
 - For example, Q3D DC bias + RF Loss for 5G RF Power Amp



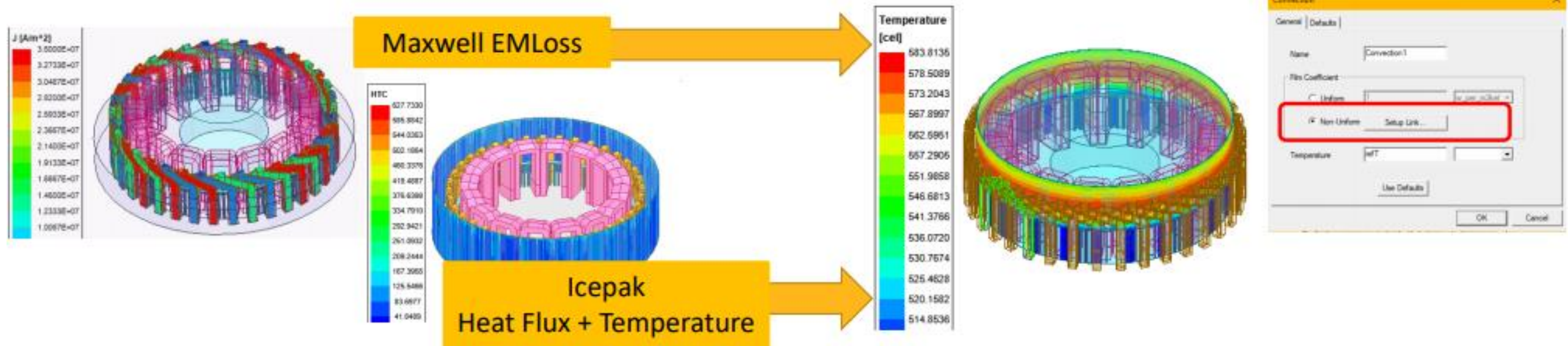
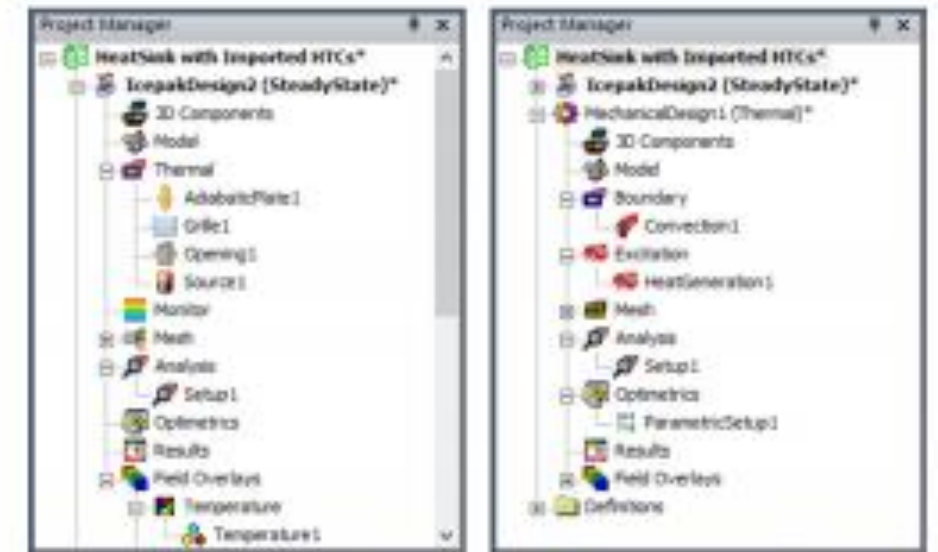
- Multiplier/Offset
 - Enable users to adjust power levels without going back to source design



- Surface losses on sheet object
- Optimetrics & 2-way thermal workflow

AEDT Mechanical-Icepak机械热转换耦合

- 使用机械热来模拟传导问题
- 使用简化的Icepak模型求解流体流动
- 单一电子桌面内的无缝集成



Thank you for your kind attention.
We are looking forward to doing business with you.



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